1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M72-EVT

03/27/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
27		495038	ENGINEERING RELEASED	03/27/07	?

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3	Power Block Diagram	03/05/2007 MARK
4	BOM Configuration	03/05/2007 JAMES
5	Revision History	03/05/2007 JAMES
6	Power Conn / Alias	03/05/2007 MARK
7	Functional / ICT Test	03/05/2007 JAMES
8	GROUNDING ALIASES	03/05/2007 MARK
9	CPU FSB	03/05/2007 JAMES
10	CPU Power & Ground	03/05/2007 JAMES
11	CPU Decoupling & VID	03/05/2007 MARK
12	eXtended Debug Port (XDP)	03/05/2007 JAMES
13	NB CPU Interface	03/05/2007 T9_MLB_NOME
14	NB PEG / Video Interfaces	03/05/2007 T9_MLB_NOME
15	NB Misc Interfaces	03/05/2007 T9_MLB_NOME
16	NB DDR2 Interfaces	03/05/2007 T9_MLB_NOME
17	NB Power 1	03/05/2007 T9_MLB_NOME
18	NB Power 2	03/05/2007 T9_MLB_NOME
19	NB Grounds	03/05/2007 T9_MLB_NOME
20	NB Standard Decoupling	03/05/2007 JAMES
21	NB Graphics Decoupling	03/05/2007 JAMES
22	SB Enet, Disk, FSB, LPC	03/05/2007 DAVE
23	SB PCI, PCIe, DMI, USB	03/05/2007 DAVE
24	SB Pwr Mgt, GPIO, Clink	03/05/2007 DAVE
25	SB Power & Ground	03/05/2007 DAVE
26	SB Decoupling	03/05/2007 DAVE
27	SB Misc	03/05/2007 DAVE
28	Clock (CK505)	03/05/2007 JAMES
29	Clock Termination	03/05/2007 JAMES
30	DDR2 SO-DIMM Connector A	03/05/2007 JAMES
31	DDR2 SO-DIMM Connector B	03/05/2007 JAMES
32	Memory Active Termination	03/05/2007 JAMES
33	PCI-E MiniCard Connector	03/05/2007 DOUG
34	Ethernet (Yukon)	03/05/2007 DOUG
35	YUKON/ULTRA SUPPORT	03/05/2007 DOUG
36	ETHERNET CONNECTOR	03/05/2007 DOUG
37	FW: 1394B CONTROLLER	03/05/2007 DOUG
38	FW: 1394B MISC	03/05/2007 DOUG
39	FIREWIRE CONNECTORS	03/05/2007 DOUG
40	PATA Connector	03/05/2007 DAVE
41	SATA Connectors	03/05/2007 DOUG
42	EXTERNAL USB CONNECTORS	03/05/2007 DOUG
43	Internal USB Connections	03/05/2007 DOUG
44	SMC	03/05/2007 DAVE
45	SMC Support	03/05/2007 DAVE
46	LPC+ Debug Connector	03/05/2007 DAVE
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49	Thermal Sensors	03/05/2007 DAVE
50	HD AND OD FAN	03/05/2007 DAVE
51	CPU FAN	03/05/2007 DAVE
52	ALS Support	03/05/2007 DAVE
53	SPI BootROM	03/05/2007 DAVE
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57	IMVP6 3RD PHASE	03/05/2007 MARK
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PRELIMINARY

DRAWING
TITLE=M72
ABBREV=DRAWING
LAST_MODIFIED=Tue Mar 27 11:00:09 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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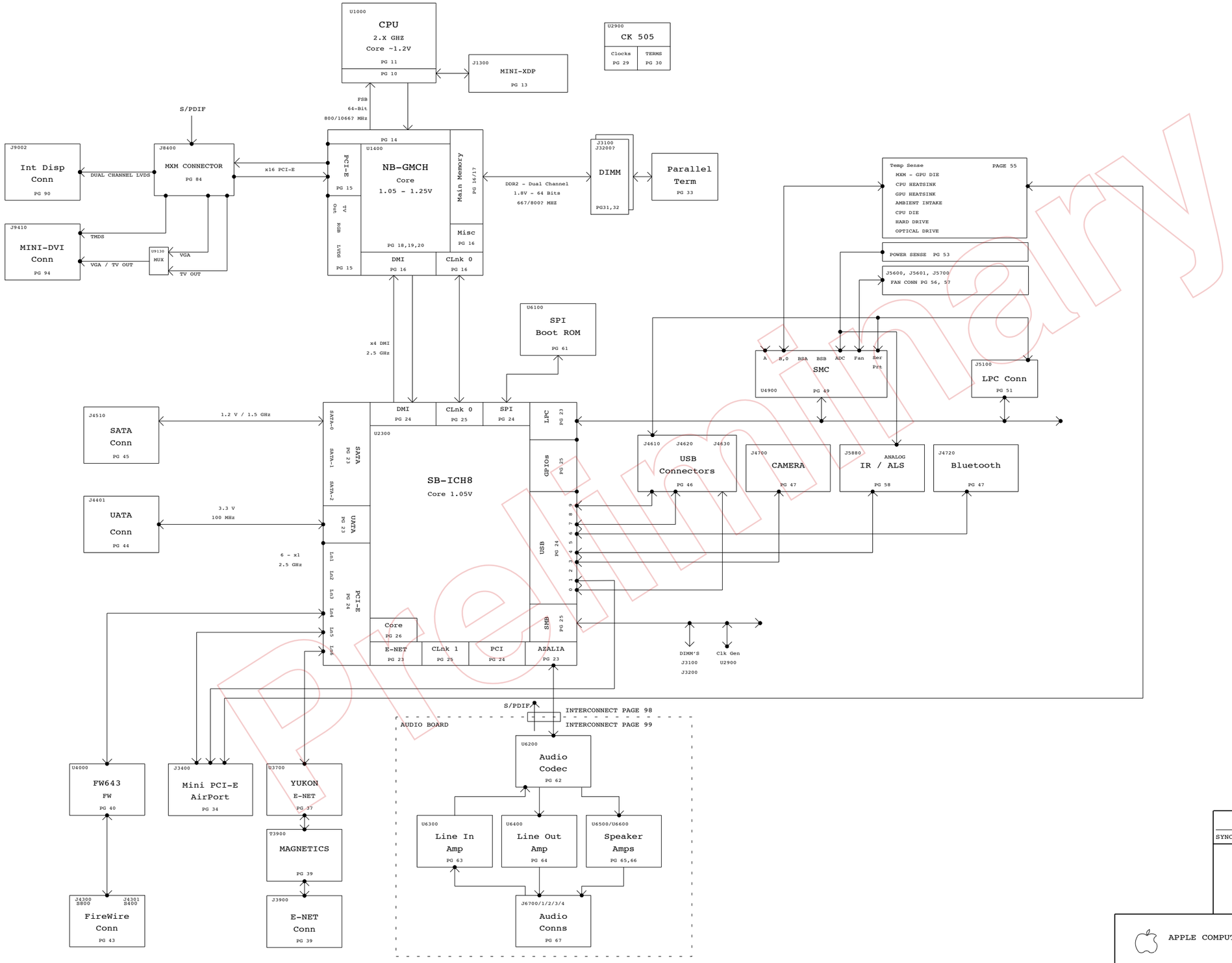
TITLE
SCH,M72,MLB

DRAWING NUMBER 051-7228 REV. 27

SHT 1 OF 118



Preliminary

System Block Diagram

SYNC_MASTER=DEREK SYNC_DATE=1/19/2007

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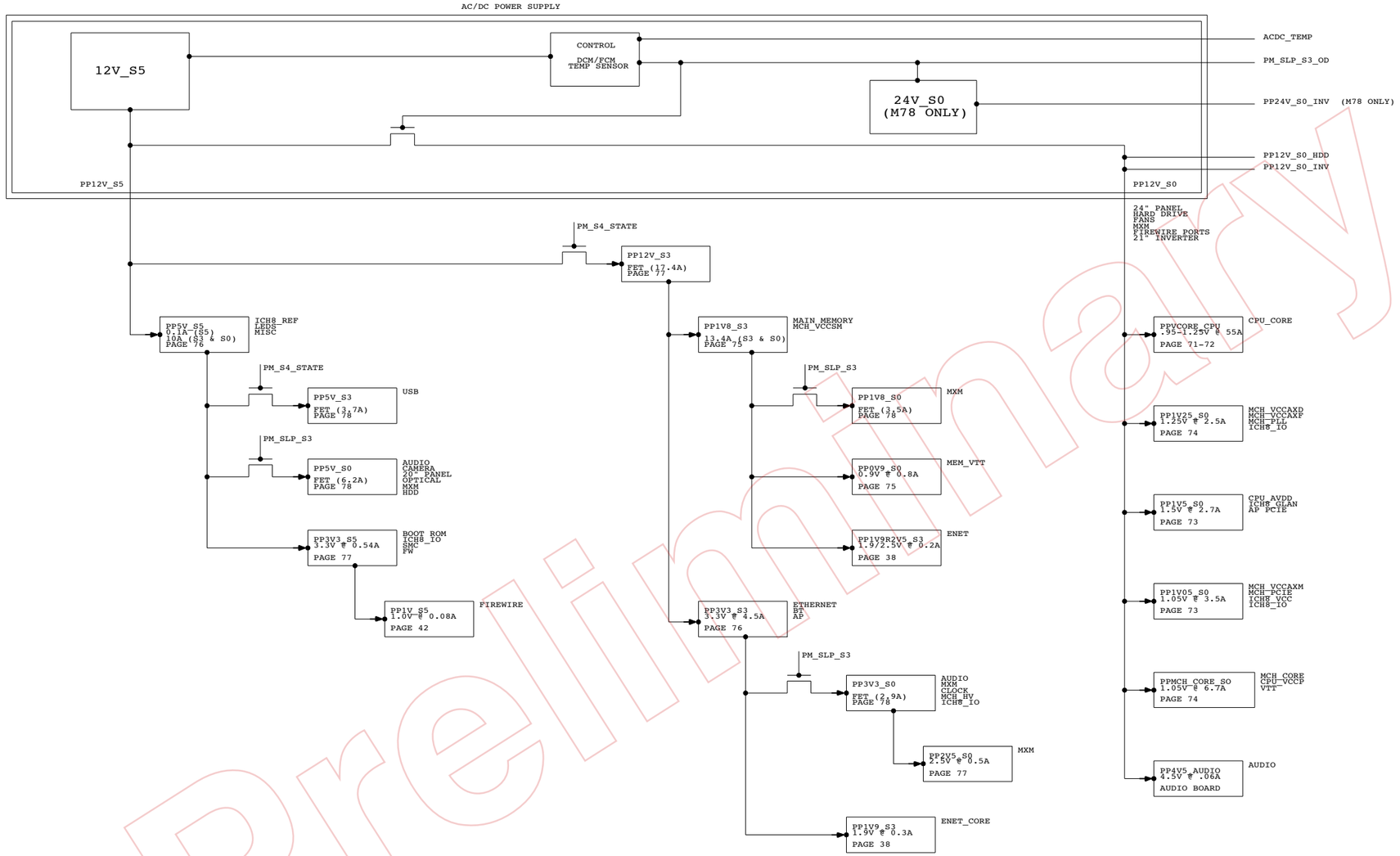
SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
NONE	2	118



Preliminary

Power Block Diagram

SYNC_MASTER=MARK SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 3 OF 118	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7977	PCBA,MLB,M78,CTO,2.8G	24_INCH_LCD,2P8GHZ_CPU,BASIC,CR_E,V8
630-7976	PCBA,MLB,M78,BTR,2.4G	24_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6
630-7875	PCBA,MLB,M78,CTO,2.2G	24_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6
607-0429	M78 DEVELOPMENT	CPU_TDIODE,DEVELOPMENT,XDP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE
630-7979	PCBA,MLB,M72,CTO,2.4G	20_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6
630-7978	PCBA,MLB,M72,BTR,2.2G	20_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6
630-7874	PCBA,MLB,M72,GD,2.0G	20_INCH_LCD,2P0GHZ_CPU,BASIC,CR_STD,V6
607-0462	M72 DEVELOPMENT	CPU_TDIODE,DEVELOPMENT,ITP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	5V1V8REG_SKIP,ALTERNATE,COMMON,ITP/XDP,MXM_ROM,NBCFG_PEG_REVERSE,YUKON_ULTRA
V6	LOW_TDP
V8	HIGH_TDP

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0381 - GM965	338S0430	1	IC,NB,CRESTLINE,PM,C0,QS	U1400	CRITICAL	
	338S0427	1	IC,SB,ICH8M,B1,QS	U2300	CRITICAL	
537 - 359S0127	359S0130	1	CK505 - SILEGO SLG2AP101	U2900	CRITICAL	
DIFFERENT FOR M787	820-2149	1	PCB,FAB,IO ALIGNMENT,M72	IO1	CRITICAL	
	069-2046	1	M72/M78 22UF CAP INTERCHANGEABILITY	DOC1		
	825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
M51 - NEED NEW P/N (335S0155 - BLNK)	341S1892	1	IC,2K I2C EEPROM,MXM	U8570	CRITICAL	MXM_ROM

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7229	1	PCB,SCHEM,MLB,M78	SCH1		24_INCH_LCD
056-XXXX (MCO) 057-XXXX (PANEL)	820-2110	1	PCB,FAB,MLB,M78,HF	MLB1		24_INCH_LCD
341T0048 = M78 EFI ROM (341S1904 - DEV) (341S1905 - PVT) (335S0384 - BLNK)						
(341S2066 - PROG) (338S0274 - BLNK)	341T0049	1	IC,SMC,M78	U4900	CRITICAL	24_INCH_LCD
	114S0292	1	RES,5.76K,0402,1%,1/16W,LF	R7117		24_INCH_LCD
	132S0010	1	CAP,CER,390PF,10%,50V,0402	C7113		24_INCH_LCD
	132S0101	1	CAP,CER,0.33UF,10%,6.3V,0402	C7128		24_INCH_LCD
	132S0131	1	CAP,CER,0.033UF,10%,16V,0402	C7134		24_INCH_LCD

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7228	1	PCB,SCHEM,MLB,M72	SCH1		20_INCH_LCD
056-2161 (MCO) 057-0399 (PANEL)	820-2143	1	PCB,FAB,MLB,M72,HF	MLB1		20_INCH_LCD
(341SXXXX - PVT) (335S0384 - BLNK)	341T0056	1	EFI ROM,M72/M78	U6100	CRITICAL	
(341S2069 - PROG) (338S0274 - BLNK)	341T0055	1	IC,SMC,M72	U4900	CRITICAL	20_INCH_LCD
	114S0309	1	RES,8.66K,0402,1%,1/16W,LF	R7117		20_INCH_LCD
	132S0205	1	CAP,CER,270PF,10%,50V,0402	C7113		20_INCH_LCD
	132S0103	1	CAP,CER,0.22UF,10%,6.3V,0402	C7128		20_INCH_LCD
	132S0070	1	CAP,CER,0.015UF,10%,16V,0402	C7134		20_INCH_LCD

337S3438	1	IC,MDC,SR,E1,QS,2.8G,55W,800FSB,4M,PGA	CPU	CRITICAL	2P8GHZ_CPU
337S3436	1	IC,MDC,SR,E1,QS,2.6G,45W,800FSB,4M,PGA	CPU	CRITICAL	2P6GHZ_CPU
337S3435	1	IC,MDC,SR,E1,QS,2.4G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P4GHZ_CPU
337S3461	1	IC,MDC,SR,E1,QS,2.2G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P2GHZ_CPU
337S3460	1	IC,MDC,SR,E1,QS,2.0G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P0GHZ_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3437	337S3436		CPU	CPU,2.6G,55W
124-0361	124-0339		C7490,C7491	CAP
371S0464	371S0154		D7624,D7664	DIODES

MXM_PWR_SENSE BOMOPTION CHANGE FOR PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0070	1	RES,0-OHM,2512	R5350		PRODUCTION
116S0090	2	RES,10K-OHM,5%,0402	C5358,C5359		PRODUCTION

BOM Configuration

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

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SIZE D | DRAWING NUMBER 051-7228 | REV. 27

SCALE NONE | SHT 4 OF 118

Preliminary

PROTO REVIEW - 11/09/06

Preliminary

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27

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
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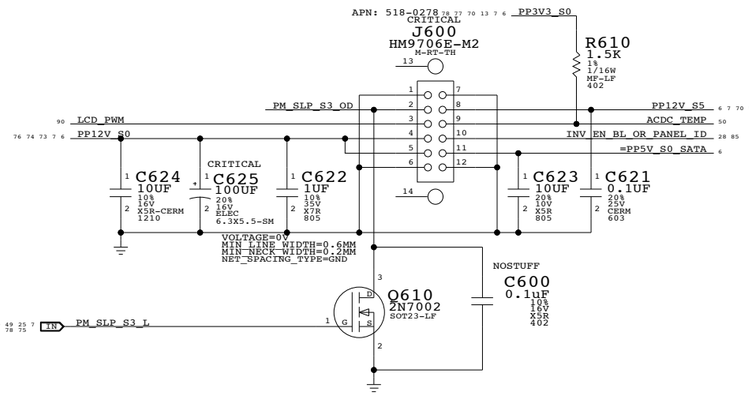

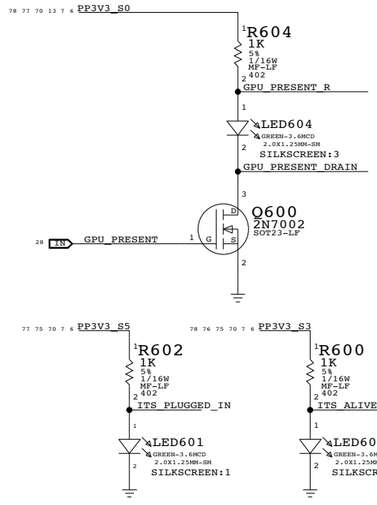

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0082	1	RES,MF,1/10W,910OHM,5,0603,SMD,LF	R605		20_INCH_LCD
113S0095	1	RES,MF,1/10W,3.3KOHM,5,0603,SMD,LF	R605		24_INCH_LCD

"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 (MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP0V9_S0M_MEM_TERM 33
- PPVCORE_CPU (MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, NET_SPACING_TYPE=PWR, MIN_NECK_WIDTH=0.3MM, MAX_NECK_LENGTH=3 MM)
  - =PPVCORE_S0_CPU 11 12 53
- PP1V8_S0 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP1V8_S0_MXM 84
- PP2V5_S0 (MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP2V5_S0_MXM 85
- PPMCH_CORE_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PPVCORE_S0_NB 18 21
  - =PPVCORE_S0_NB_FOLLOW 21
  - =PP1V05_S0_CPU 10 11 12 13 50
  - =PP1V25R1V05_S0_FSB_NB 14 30
  - =PP1V25R1V05_S0_NB_VTT 19 21
  - =PP1V05_S0_SB_CPU_IO 23 26 27
- PP1V05_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP1V05_S0M_NB_VCCAXM 18 21
  - =PP1V05_S0_NB_PCIE 21
  - =PP1V05_S0_NB_FOLLOW 21
  - =PPVCORE_S0_SB 26 27
- PP1V5_S0 (MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP1V5_S0_CPU 11 12
  - =PP1V5_S0_NB_TVDAC 22
  - =PP1V5_S0_SB_VCC1_5_A_ARX 26 27
  - =PP1V5_S0_SB_VCC1_5_A_ATX 26 27
  - =PP1V5_S0_SB_VCCUSBPLL 26 27
  - =PP1V5_S0_SB_VCC1_5_A_USB_CORE 26 27
  - =PP1V5_S0_SB_VCC1_5_A 26
  - =PP1V5_S0_SB 27
  - =PP1V5_S0_MINI 34
- PP1V25_S0 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.25V, MAKE_BASE=TRUE, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP1V25_S0_NB_VCCDMI 19 21
  - =PP1V25_S0M_NB_VCCA 21
  - =PP1V25_S0M_NB_VCC 21
  - =PP1V25_S0_NB_PLL 21
  - =PP1V25_S0_NB_VCC 21
  - =PP1V25_S0M_NB_PLL 21
  - =PP1V25_S0_SB_DMI 26 27
- PP3V3_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP3V3_S0_NB_VCCHV 16 19 21
  - =PP3V3_S0_SB 27
  - =PP3V3_S0_SB_GPIO 23 25
  - =PP3V3_S0_SB_VCCGLAN3_3 26
  - =PP3V3_S0_SB_VCC3_3_PCI 26 27
  - =PP3V3_S0_SB_VCC3_3_IDE 26 27
  - =PP3V3_S0_SB_PCI 24
  - =PP3V3_S0_SB_PM 28
  - =PP3V3_S0_PATA 44
  - =PP3V3_S0_FAN 56 57
  - =PPSPD_S0_MEM 31 32
  - =PP3V3_S0_IMVP 71
  - =PP3V3_S0_AUDIO 98
  - =PP3V3_S0_LPCPLUS 51
  - =PP3V3_S0_SMBUS_SB 52
  - =PP3V3_S0_SMC_LS 50
  - =PP3V3_S0_SMBUS_SMC_0_S0 52
  - =PP3V3_S0_SMBUS_SMC_B_S0 52
  - =PP3V3_S0_SMBUS_SMC_MGMT 52
  - =PP3V3_S0_CK505 29 30
  - =PP3V3_S0_MXM 85
  - =PP3V3_S0_SATALED 45
  - =PP3V3_S0M_CK505 29 30
  - =PP3V3_S0MWOL_SB_CLINK0 25
  - =PP3V3_S0_SB_VCC3_3_DMI 26 27
  - =PP3V3_S0_SB_VCC3_3_SATA 26 27
  - =PP3V3_S0_SB_VCC3_3_VCCPCORE 26
  - =PP3V3R1V5_S0_SB_VCCHDA 26 27
  - =PP3V3_S0MWOL_SB_VCCLAN3_3 26 27
  - =PP3V3_S0MWOL_SB_VCCCL3_3 26 27
  - =PP3V3_S0_TSENS 55
  - =PP3V3_S0_SMC 53
  - =PP3V3_S0_NB_VCCA_PEG_BG 19 21
  - =PP3V3_S0_NB_FOLLOW 21
  - =PP3V3_S0_VIDEO 90 91 94
  - =PP3V3_S0_ENET 38
- PP5V_S0 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP5V_S0_SB 27
  - =PP5V_S0_PATA 44
  - =PP5V_S0_LPCPLUS 7 51
  - =PP5V_S0_AUDIO 98
  - =PP5V_S0_SATA 6
  - =PP5V_S0_MXM 84
  - =PPV_S0_LCD_20INCH 90
- PP12V_S0 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP12V_S0_FAN 56 57
  - =PP12V_S0_AUDIO_SPKRAMP 98
  - =PP12V_S0_CPU 53 71 72
  - =PPV_S0_LCD_24INCH 90
  - =PPV_S0_MXM_PWRSRC 53

"S3" RAILS

ON IN RUN AND SLEEP

- PP1V8_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP1V8_S3M_MEM_NB 16 18 21 22
  - =PP1V8_S3M_NB_VCC 21
  - =PP1V8_S3_MEM 31 32
  - =PP1V8_S3_MEMVTT 75
  - =PP1V8_S3_ENET 38
- PP3V3_S3 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP3V3_S3_MINI 34
  - =PP3V3_S3_ENET 38 39
  - =PP3V3_S3_BT 47
- PP5V_S3 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP5V_S3_BNDI 47 58
  - =PP5V_S3_MEMVTT 75
  - =PP5V_S3_SYSLED 50
  - =PP5V_S3_ALS 58

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

- PP3V3_S5 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP3V3_S5_SB 25 27 28
  - =PP3V3_S5_SB_USB 24
  - =PP3V3_S5_SB_PM 28
  - =PP3V3_S5_SB_VCCSUS3_3 26 27
  - =PP3V3_S5_SB_VCCSUS3_3_USB 26 27
  - =PP3V3_S5_SMBUS_SB_ME 52
  - =PP3V3_S5_FW 40 42 43
  - =PP3V3_S5_SMC 49 50
  - =PP3V3_S5_ROM 61
  - =PP3V3_S5_SB_GPIO 25
  - =PP3V3_S5_SB_CLINK1 25
  - =PP3V3_S5_SB_3V3_VCCSUSHDA 26 27
  - =PP3V3_S5_LPCPLUS 7 51
  - =PP3V3_S5_SMBUS_SMC_BSA 52
  - =PP3V3_S5_FAN 56 57
  - =PP3V3_S5_SMCUSBMUX 46
  - =PP3V3_S5_SMBUS_SMC_A_S5 52
- PP5V_S5 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP5V_S5_SB 27
  - =PPVIN_S5_SMCVREF 50
  - =PP5V_S5_USB 46
- PP12V_S5 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
  - =PP12V_S5_FET 78
  - =PP12V_S5_FW 43

Power Conn / Alias

SYNC_MASTER=MARK SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 6 OF 118	

Preliminary

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

100 14 10 7	FSB_A_L<6>	PP1000	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1001	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1002	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1003	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1004	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1005	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1006	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1007	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1008	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1009	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1010	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1011	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1012	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1013	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1014	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1015	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1016	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1017	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1018	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1019	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1020	OMIT P4MM
100 14 13 10	FSB_CPURST_L	PP1021	OMIT P4MM
100 51 23 10	CPU_INIT_L	PP1022	OMIT P4MM
100 23 10	CPU_A20M_L	PP1023	OMIT P4MM
100 23 10	CPU_IGNNE_L	PP1024	OMIT P4MM
100 23 10	CPU_STPCLK_L	PP1025	OMIT P4MM
100 23 10	CPU_INTR	PP1026	OMIT P4MM
100 23 10	CPU_NMI	PP1027	OMIT P4MM
100 23 10	CPU_SMI_L	PP1028	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1029	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1030	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1031	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1032	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1033	OMIT P4MM
105 30 10	FSB_CLK_CPU_P	PP1034	OMIT P4MM
105 30 10	FSB_CLK_CPU_N	PP1035	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

105 30 23	SB_CLK100M_SATA_P	PP2100	OMIT P4MM
105 30 23	SB_CLK100M_SATA_N	PP2101	OMIT P4MM
103 44 23	IDE_PDIOR_L	PP2102	OMIT P4MM
103 44 23	IDE_PDIORDY	PP2103	OMIT P4MM
103 44 23	IDE_PDD<9>	PP2104	OMIT P4MM
104 34 24	PCIE_MINI_D2R_P	PP2105	OMIT P4MM
104 34 24	PCIE_MINI_D2R_N	PP2106	OMIT P4MM
104 37 24	PCIE_ENET_D2R_P	PP2107	OMIT P4MM
104 37 24	PCIE_ENET_D2R_N	PP2108	OMIT P4MM
104 42 40	PCIE_FW_D2R_P	PP2132	OMIT P4MM
104 42 40	PCIE_FW_D2R_N	PP2133	OMIT P4MM
101 24 16	DMI_N2S_P<0>	PP2109	OMIT P4MM
101 24 16	DMI_N2S_N<0>	PP2110	OMIT P4MM
105 30 24 7	SB_CLK100M_DMI_P	PP2111	OMIT P4MM
105 30 24 7	SB_CLK100M_DMI_N	PP2112	OMIT P4MM
49 28 25	PM_SYSRST_L	PP2113	OMIT P4MM
51 49 25 7	PM_CLKRUN_L	PP2114	OMIT P4MM
105 30 25	SB_CLK14P3M_TIMER	PP2115	OMIT P4MM
105 30 25	SB_CLK48M_USBCTLR	PP2116	OMIT P4MM
105 30 24	PCI_CLK33M_SB	PP2117	OMIT P4MM
28 23 7	SB_RTC_RST_L	PP2118	OMIT P4MM
103 45 23	SATA_A_D2R_P	PP2119	OMIT P4MM
103 45 23	SATA_A_D2R_N	PP2120	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP2121	OMIT P4MM
103 47 24	USB_CAMERA_P	PP2122	OMIT P4MM
103 47 24	USB_CAMERA_N	PP2123	OMIT P4MM
103 47 24	USB_IR_P	PP2124	OMIT P4MM
103 47 24	USB_IR_N	PP2125	OMIT P4MM
103 47 24	USB_BT_P	PP2126	OMIT P4MM
103 47 24	USB_BT_N	PP2127	OMIT P4MM
103 61 24	SPI_SCLK_R	PP2128	OMIT P4MM
103 61 24	SPI_SO	PP2129	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP2130	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP2131	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1400

100 14 10 7	FSB_A_L<6>	PP1400	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1401	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1402	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1403	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1404	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1405	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1406	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1407	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1408	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1409	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1410	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1411	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1412	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1413	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1414	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1415	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1416	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1417	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1418	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1419	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1420	OMIT P4MM
100 14 10	FSB_HIT_L	PP1421	OMIT P4MM
100 14 10	FSB_HITM_L	PP1422	OMIT P4MM
100 14 10	FSB_BNR_L	PP1423	OMIT P4MM
100 14 10	FSB_BREQ0_L	PP1424	OMIT P4MM
100 14 10	FSB_DBSY_L	PP1425	OMIT P4MM
100 14 10	FSB_DPWR_L	PP1426	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1427	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1428	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1429	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1430	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1431	OMIT P4MM
105 30 14	FSB_CLK_NB_P	PP1432	OMIT P4MM
105 30 14 7	FSB_CLK_NB_N	PP1433	OMIT P4MM
71 70 22 16 7	VR_PWRGOOD_DELAY	PP1434	OMIT P4MM
28 16	NB_RESET_L	PP1435	OMIT P4MM
105 30 16	NB_CLK100M_PCIE_P	PP1436	OMIT P4MM
105 30 16 7	NB_CLK100M_PCIE_N	PP1437	OMIT P4MM
101 24 16	DMI_S2N_N<0>	PP1438	OMIT P4MM
101 24 16	DMI_S2N_P<0>	PP1439	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFA	PP1440	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFB	PP1441	OMIT P4MM
102 31 17	MEM_A_DQ<7>	PP1442	OMIT P4MM
102 31 17	MEM_A_DQ<14>	PP1443	OMIT P4MM
102 31 17	MEM_A_DQ<16>	PP1444	OMIT P4MM
102 31 17	MEM_A_DQ<25>	PP1445	OMIT P4MM
102 31 17	MEM_A_DQ<39>	PP1446	OMIT P4MM
102 31 17	MEM_A_DQ<47>	PP1447	OMIT P4MM
102 31 17	MEM_A_DQ<54>	PP1448	OMIT P4MM
102 31 17	MEM_A_DQ<59>	PP1449	OMIT P4MM
102 31 17	MEM_A_DQS_P<0>	PP1450	OMIT P4MM
102 31 17	MEM_A_DQS_N<0>	PP1451	OMIT P4MM
102 31 17	MEM_A_DQS_P<1>	PP1452	OMIT P4MM
102 31 17	MEM_A_DQS_N<1>	PP1453	OMIT P4MM
102 31 17	MEM_A_DQS_P<2>	PP1454	OMIT P4MM
102 31 17	MEM_A_DQS_N<2>	PP1455	OMIT P4MM
102 31 17	MEM_A_DQS_P<3>	PP1456	OMIT P4MM
102 31 17	MEM_A_DQS_N<3>	PP1457	OMIT P4MM
102 31 17	MEM_A_DQS_P<4>	PP1458	OMIT P4MM
102 31 17	MEM_A_DQS_N<4>	PP1459	OMIT P4MM
102 31 17	MEM_A_DQS_P<5>	PP1460	OMIT P4MM
102 31 17	MEM_A_DQS_N<5>	PP1461	OMIT P4MM
102 31 17	MEM_A_DQS_P<6>	PP1462	OMIT P4MM
102 31 17	MEM_A_DQS_N<6>	PP1463	OMIT P4MM
102 31 17	MEM_A_DQS_P<7>	PP1464	OMIT P4MM
102 31 17	MEM_A_DQS_N<7>	PP1465	OMIT P4MM
102 32 17	MEM_B_DQ<6>	PP1466	OMIT P4MM
102 32 17	MEM_B_DQ<8>	PP1467	OMIT P4MM
102 32 17	MEM_B_DQ<23>	PP1468	OMIT P4MM
102 32 17	MEM_B_DQ<25>	PP1469	OMIT P4MM
102 32 17	MEM_B_DQ<38>	PP1470	OMIT P4MM
102 32 17	MEM_B_DQ<44>	PP1471	OMIT P4MM
102 32 17	MEM_B_DQ<48>	PP1472	OMIT P4MM
102 32 17	MEM_B_DQ<62>	PP1473	OMIT P4MM
102 32 17	MEM_B_DQS_P<0>	PP1474	OMIT P4MM
102 32 17	MEM_B_DQS_N<0>	PP1475	OMIT P4MM
102 32 17	MEM_B_DQS_P<1>	PP1476	OMIT P4MM
102 32 17	MEM_B_DQS_N<1>	PP1477	OMIT P4MM
102 32 17	MEM_B_DQS_P<2>	PP1478	OMIT P4MM
102 32 17	MEM_B_DQS_N<2>	PP1479	OMIT P4MM
102 32 17	MEM_B_DQS_P<3>	PP1480	OMIT P4MM
102 32 17	MEM_B_DQS_N<3>	PP1481	OMIT P4MM
102 32 17	MEM_B_DQS_P<4>	PP1482	OMIT P4MM
102 32 17	MEM_B_DQS_N<4>	PP1483	OMIT P4MM
102 32 17	MEM_B_DQS_P<5>	PP1484	OMIT P4MM
102 32 17	MEM_B_DQS_N<5>	PP1485	OMIT P4MM
102 32 17	MEM_B_DQS_P<6>	PP1486	OMIT P4MM
102 32 17	MEM_B_DQS_N<6>	PP1487	OMIT P4MM
102 32 17	MEM_B_DQS_P<7>	PP1488	OMIT P4MM
102 32 17	MEM_B_DQS_N<7>	PP1489	OMIT P4MM
101 84 15	PEG_D2R_P<7>	PP1490	OMIT P4MM
101 84 15	PEG_D2R_N<7>	PP1491	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP1492	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP1493	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U3700

105 37 30	PCIE_CLK100M_ENET_P	PP3700	OMIT P4MM
105 37 30	PCIE_CLK100M_ENET_N	PP3701	OMIT P4MM
108 37	PCIE_ENET_R2D_P	PP3702	OMIT P4MM
108 37	PCIE_ENET_R2D_N	PP3703	OMIT P4MM
37 28	ENET_RESET_L	PP3704	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4000

105 40 30	PCIE_CLK100M_FW_P	PP4000	OMIT P4MM
105 40 30	PCIE_CLK100M_FW_N	PP4001	OMIT P4MM
108 40	PCIE_FW_R2D_P	PP4002	OMIT P4MM
108 40	PCIE_FW_R2D_N	PP4003	OMIT P4MM
40 28 7	FW_RESET_L	PP4004	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4900

105 49 30	PCI_CLK33M_SMC	PP4900	OMIT P4MM
49 28	SMC_LRESET_L	PP4901	OMIT P4MM
51 50 49 7	SMC_RESET_L	PP4902	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP4903	OMIT P4MM

LPC CONNECTOR

51 6	=PP3V3_S5_LPCPLUS	FUNC_TEST=TRUE
51 6	=PP5V_S0_LPCPLUS	FUNC_TEST=TRUE
105 51 30	FWH_INIT_L	FUNC_TEST=TRUE
51 49 23	PCI_CLK33M_LPCPLUS	FUNC_TEST=TRUE
51 49 23 7	LPC_AD<0>	FUNC_TEST=TRUE
51 49 23 7	LPC_AD<1>	FUNC_TEST=TRUE
51 49 23	LPC_AD<2>	FUNC_TEST=TRUE
51 49 23	LPC_AD<3>	FUNC_TEST=TRUE
51 49 23	LPC_FRAME_L	FUNC_TEST=TRUE
51 49 25 7	PM_CLKRUN_L	FUNC_TEST=TRUE
51 24	BOOT_LPC_SPI_L	FUNC_TEST=TRUE
51 50 49	SMC_TMS	FUNC_TEST=TRUE
51 28	DEBUG_RESET_L	FUNC_TEST=TRUE
51 49	SMC_TRST_L	FUNC_TEST=TRUE
51 50 49	SMC_TDO	FUNC_TEST=TRUE
51 49	SMC_MD1	FUNC_TEST=TRUE
51 50 49 46	SMC_TX_L	FUNC_TEST=TRUE
51 49 25	INT_SERIRQ	FUNC_TEST=TRUE
51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE
51 50 49	SMC_TDI	FUNC_TEST=TRUE
51 50 49	SMC_TCK	FUNC_TEST=TRUE
51 50 49 7	SMC_RESET_L	FUNC_TEST=TRUE
51 49	SMC_NMI	FUNC_TEST=TRUE
51 50 49 46	SMC_RX_L	FUNC_TEST=TRUE
51 25	LINDACARD_GPIO	FUNC_TEST=TRUE
	16 TP'S	
		FUNC_TEST=TRUE

PWROK SEQUENCING

84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE

STARTUP (BOOT/WAKE) TIMING

71 49	IMVP_VR_ON	FUNC_TEST=TRUE
28 25	VR_PWRGD_CLKEN	FUNC_TEST=TRUE
71 70 22 16 7	VR_PWRGOOD_DELAY	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE

SHUTDOWN/SLEEP TIMING

51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE
78 75 70 49 25 6	PM_SLP_S3_L	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE
84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE
100 23 13 10	CPU_PWRGD	FUNC_TEST=TRUE

"S0" RAILS

75 70 6	PPDV9_S0	FUNC_TEST=TRUE
72 71 6	PPVCORE_CPU	FUNC_TEST=TRUE
78 70 6	PP1V8_S0	FUNC_TEST=TRUE
77 6	PP2V5_S0	FUNC_TEST=TRUE
74 73 55 6	PPMCH_CORE_S0	FUNC_TEST=TRUE
73 34 6	PP1V05_S0	FUNC_TEST=TRUE
74 6	PP1V25_S0	FUNC_TEST=TRUE
78 77 70 13 6	PP3V3_S0	FUNC_TEST=TRUE
94 78 74 73 72 71 70 6	PP5V_S0	FUNC_TEST=TRUE
	3 TP'S	
76 74 73 6	PP12V_S0	FUNC_TEST=TRUE
73 6	PP1V5_S0	FUNC_TEST=TRUE

"S3" RAILS

	3 TP'S	
78 76 75 50	PP12V_S3	FUNC_TEST=TRUE
78 75 6	PP1V8_S3	FUNC_TEST=TRUE
78 76 75 70 6	PP3V3_S3	FUNC_TEST=TRUE
78 76 75 70 6	PP5V_S3	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE

"S5" RAILS

	3 TP'S	
77 75 70 6	PP3V3_S5	FUNC_TEST=TRUE
78 77 76 70 6	PP5V_S5	FUNC_TEST=TRUE
	5 TP'S	
78 76 70 6	PP12V_S5	FUNC_TEST=TRUE

FOR ICT

105 30 16 7	NB_CLK100M_PCIE_N	FUNC_TEST=TRUE
105 30 14 7	FSB_CLK_NB_N	FUNC_TEST=TRUE
16	TP_NB_CFG<13>	FUNC_TEST=TRUE
16	TP_NB_CFG<12>	FUNC_TEST=TRUE
16	TP_NB_CFG<18>	FUNC_TEST=TRUE
16	NB_CFG<19>	FUNC_TEST=TRUE
104 24	PCI_REQ1_L	FUNC_TEST=TRUE
104 24	PCI_REQ2_L	FUNC_TEST=TRUE
105 30 24 7	SB_CLK100M_DMI_N	FUNC_TEST=TRUE
30	TP_CK505_REF1	FUNC_TEST=TRUE
30	TP_CK505_PCI1_CLK	FUNC_TEST=TRUE
40	TP_FW_TCK	FUNC_TEST=TRUE
40	TP_FW_TMS	FUNC_TEST=TRUE
40	TP_FW_TDI	FUNC_TEST=TRUE
40	TP_FW_TDO	FUNC_TEST=TRUE
40	FW_TRST_L	FUNC_TEST=TRUE
40	TP_FW_SM	FUNC_TEST=TRUE
40	TP_FW_SE	FUNC_TEST=TRUE
40	TP_FW_NAND_TREE	FUNC_TEST=TRUE
40	TP_FW_CE	FUNC_TEST=TRUE
103 61	SPI_CE_L<0>	FUNC_TEST=TRUE
103 61	SPI_A_SO_R	FUNC_TEST=TRUE
16	TP_NB_RSVD<12>	FUNC_TEST=TRUE
16	TP_NB_RSVD<11>	FUNC_TEST=TRUE
16	TP_NB_RSVD<13>	FUNC_TEST=TRUE
16	TP_NB_RSVD<10>	FUNC_TEST=TRUE
16 13	NB_CFG<3>	FUNC_TEST=TRUE
16 13	NB_CFG<4>	FUNC_TEST=TRUE
16 13	NB_CFG<5>	FUNC_TEST=TRUE
16 13	NB_CFG<6>	FUNC_TEST=TRUE
16 13	NB_CFG<7>	FUNC_TEST=TRUE
22	TP_LVDS_BKLT_EN	FUNC_TEST=TRUE
103 44 24	ODD_RST_5VTOL_L	FUNC_TEST=TRUE
28 23 7	SB_RTC_RST_L	FUNC_TEST=TRUE
105 30 24 7	SB_CLK100M_DMI_P	FUNC_TEST=TRUE
40 28 7	FW_RESET_L	FUNC_TEST=TRUE
103 61	SPI_SCLK	FUNC_TEST=TRUE
37	ENET_CLK25M_XTALI	FUNC_TEST=TRUE
37	ENET_CLK25M_XTALO	FUNC_TEST=TRUE

NO TEST

16	TP_NB_NC<1>	NO_TEST=TRUE
16	TP_NB_NC<2>	NO_TEST=TRUE
16	TP_NB_NC<3>	NO_TEST=TRUE
16	TP_NB_NC<4>	NO_TEST=TRUE
16	TP_NB_NC<5>	NO_TEST=TRUE
28 23	TP_LAN_D2R<2>	NO_TEST=TRUE
34 28 25	TP_CLINK_WLAN_DATA	NO_TEST=TRUE
29	TP_CK505_PGMODE	NO_TEST=TRUE
28	TP_PCI_AD_4	NO_TEST=TRUE
104 28 24	PCI_SERR_L	NO_TEST=TRUE

MISC GROUND VIAS - NEEDED?

ZH500 HOLE-VIA, ZH510 HOLE-VIA, ZH520 HOLE-VIA
ZH501 HOLE-VIA, ZH511 HOLE-VIA, ZH521 HOLE-VIA
ZH502 HOLE-VIA, ZH512 HOLE-VIA, ZH522 HOLE-VIA
ZH503 HOLE-VIA, ZH513 HOLE-VIA, ZH523 HOLE-VIA
ZH504 HOLE-VIA, ZH514 HOLE-VIA, ZH524 HOLE-VIA
ZH505 HOLE-VIA, ZH515 HOLE-VIA, ZH525 HOLE-VIA
ZH506 HOLE-VIA, ZH516 HOLE-VIA, ZH526 HOLE-VIA
ZH507 HOLE-VIA, ZH517 HOLE-VIA, ZH527 HOLE-VIA
ZH508 HOLE-VIA, ZH518 HOLE-VIA, ZH528 HOLE-VIA
ZH509 HOLE-VIA, ZH519 HOLE-VIA, ZH529 HOLE-VIA

BTW DIMMS

SC0700 EMI-SPRING CLIP-SM1
SC0701 EMI-SPRING CLIP-SM1
SC0702 EMI-SPRING CLIP-SM1

860-0894 SDF0724 SPACER-8P0OD1P07H-TH

452-0508 SDF0726 HSK-NUT-6.5MM TH
SDF0727 HSK-NUT-6.5MM TH

998-0846 FOR NB HEATSINK
OMIT ZH0722 4R3P25
OMIT ZH0723 4R3P25
OMIT ZH0725 4R3P25

998-0850
OMIT ZH0700 4P75R4
OMIT ZH0701 4P75R4
OMIT ZH0702 4P75R4
OMIT ZH0703 4P75R4

998-0847
OMIT ZH0710 4P25R3P5
OMIT ZH0711 5R3P5-6B 998-1608
OMIT ZH0712 4P25R3P5
OMIT ZH0713 4P25R3P5
OMIT ZH0714 4P25R3P5
OMIT ZH0715 4P25R3P5

860-0895 SDF0717 STDOFF-7P0OD15P0H-TH

998-0847
OMIT ZH0718 4P25R3P5
OMIT ZH0719 4P25R3P5
OMIT ZH0720 4P25R3P5

860-0895 SDF0721 STDOFF-7P0OD15P0H-TH

Functional / ICT Test

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 7 OF 118	

Confidential

GND RAILS

98 GND_AUDIO_SPKRAMP
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=GND

CHASSIS GND

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

46 GND_CHASSIS_USB

43 GND_CHASSIS_FIREWIRE
39 GND_CHASSIS_ENET
94 =GND_CHASSIS_DVI

NOTE:
PER EMC REQUIREMENTS, ALL CHASSIS GROUNDS ARE TIED DIRECTLY TO GND

Preliminary

GROUNDING ALIASES

SYNC_MASTER=MARK SYNC_DATE=(10/02/2006)

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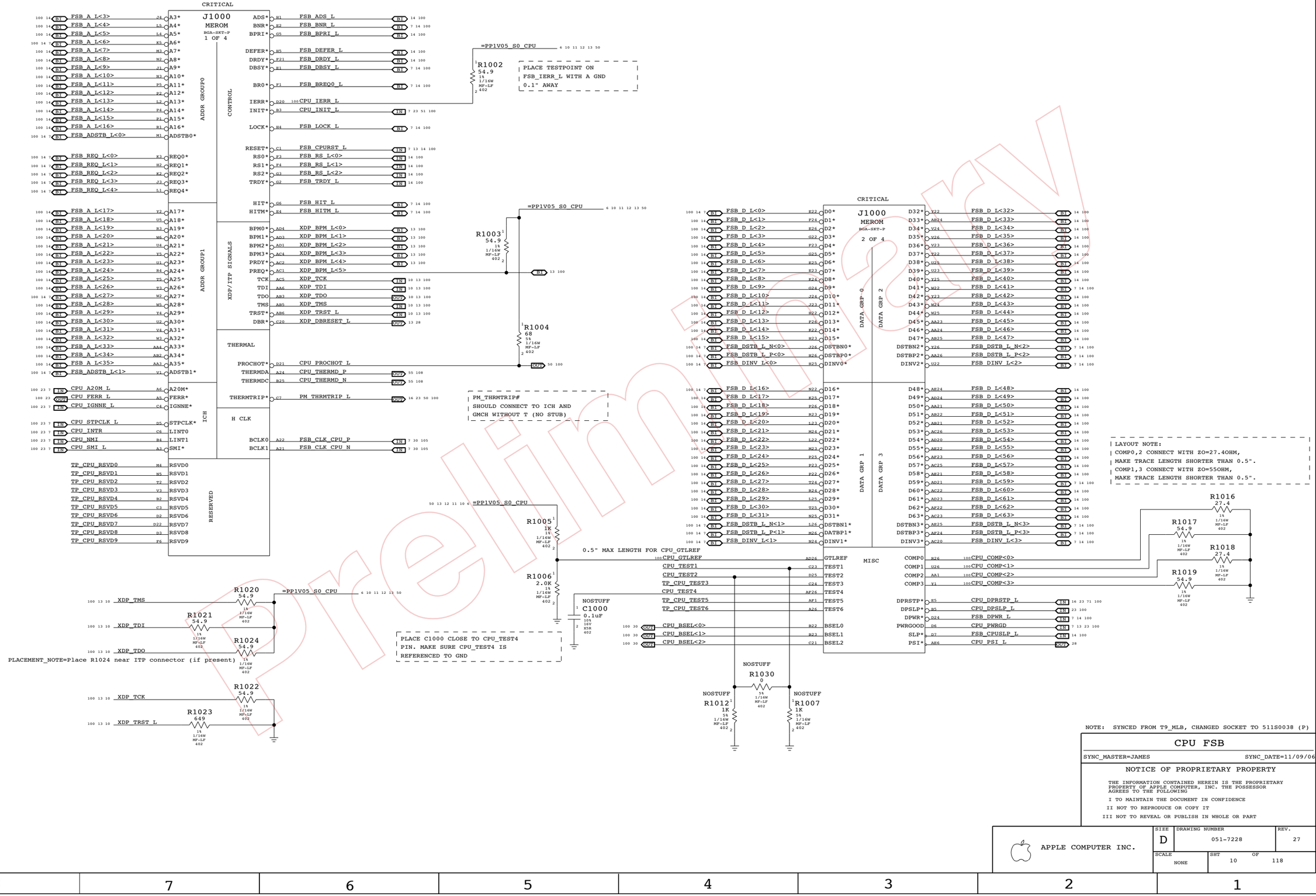
D	051-7228	27

SCALE	SHT	OF
NONE	9	118


CRITICAL
J1000
MEROM
BGA-SKT-P
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
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FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
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FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_A_L<32>
FSB_A_L<33>
FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD0
TP_CPU_RSVD1
TP_CPU_RSVD2
TP_CPU_RSVD3
TP_CPU_RSVD4
TP_CPU_RSVD5
TP_CPU_RSVD6
TP_CPU_RSVD7
TP_CPU_RSVD8
TP_CPU_RSVD9
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
NOSTUFF C1000 0.1uF 10% 16V X5R 402
0.5" MAX LENGTH FOR CPU_GTLREF
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND
R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)
CRITICAL
J1000
MEROM
BGA-SKT-P
2 OF 4
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
D0* D1* D2* D3* D4* D5* D6* D7* D8* D9* D10* D11* D12* D13* D14* D15*
D16* D17* D18* D19* D20* D21* D22* D23* D24* D25* D26* D27* D28* D29* D30* D31*
DSTBN0* DSTBP0* DINV0*
DSTBN1* DSTBP1* DINV1*
D32* D33* D34* D35* D36* D37* D38* D39* D40* D41* D42* D43* D44* D45* D46* D47*
DSTBN2* DSTBP2* DINV2*
D48* D49* D50* D51* D52* D53* D54* D55* D56* D57* D58* D59* D60* D61* D62* D63*
DSTBN3* DSTBP3* DINV3*
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6
BSEL0 BSEL1 BSEL2
COMP0 COMP1 COMP2 COMP3
DPRSTP* DPSLP* DPWR* PWRGOOD SLP* PSI*
CPU_BSEL<0> CPU_BSEL<1> CPU_BSEL<2>
CPU_COMP<0> CPU_COMP<1> CPU_COMP<2> CPU_COMP<3>
CPU_DPRSTP_L CPU_DPSLP_L FSB_DPWR_L CPU_PWRGD FSB_CPUSLP_L CPU_PSI_L
NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402
R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)
CPU FSB
SYNC_MASTER=JAMES
SYNC_DATE=11/09/06
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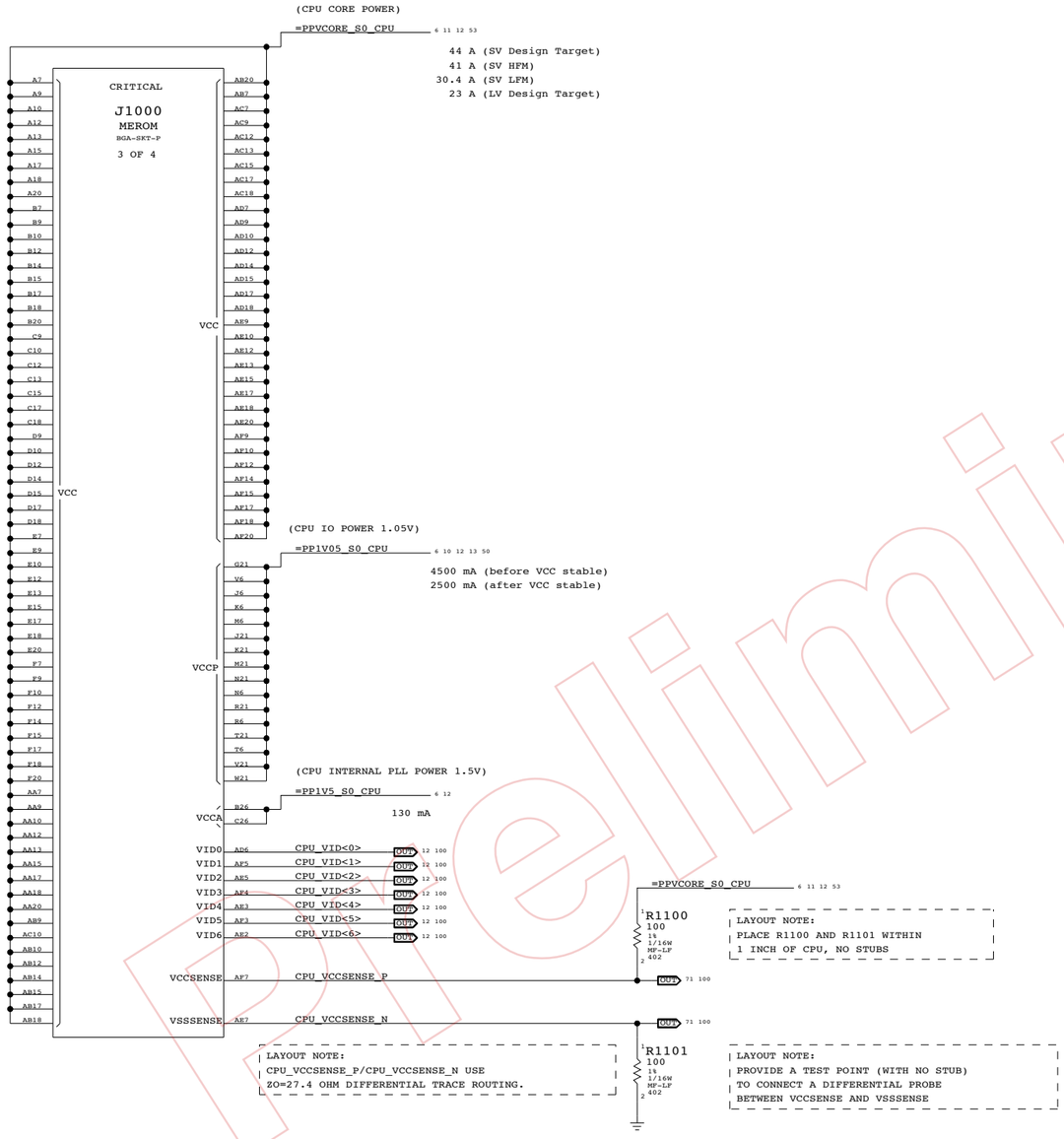
SIZE D
DRAWING NUMBER 051-7228
REV. 27
SCALE NONE
SHT 10 OF 118



Preliminary

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground

SYNC_MASTER=JAMES SYNC_DATE=11/09/06

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SCALE: NONE	SHT 11 OF 118	

CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53 11 6 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

NOSTUFF C1200 22UF 20% 6.3V X5R 805
C1201 22UF 20% 6.3V X5R 805
C1202 22UF 20% 6.3V X5R 805
C1203 22UF 20% 6.3V X5R 805
C1204 22UF 20% 6.3V X5R 805
C1205 22UF 20% 6.3V X5R 805
C1206 22UF 20% 6.3V X5R 805
C1207 22UF 20% 6.3V X5R 805
C1208 22UF 20% 6.3V X5R 805
C1209 22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210 22UF 20% 6.3V X5R 805
C1211 22UF 20% 6.3V X5R 805
C1212 22UF 20% 6.3V X5R 805
C1213 22UF 20% 6.3V X5R 805
C1214 22UF 20% 6.3V X5R 805
C1215 22UF 20% 6.3V X5R 805
C1216 22UF 20% 6.3V X5R 805
C1217 22UF 20% 6.3V X5R 805
C1218 22UF 20% 6.3V X5R 805
C1219 22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220 22UF 20% 6.3V X5R 805
C1221 22UF 20% 6.3V X5R 805
NOSTUFF C1222 22UF 20% 6.3V X5R 805
NOSTUFF C1223 22UF 20% 6.3V X5R 805
NOSTUFF C1224 22UF 20% 6.3V X5R 805
NOSTUFF C1225 22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226 22UF 20% 6.3V X5R 805
C1227 22UF 20% 6.3V X5R 805
NOSTUFF C1228 22UF 20% 6.3V X5R 805
NOSTUFF C1229 22UF 20% 6.3V X5R 805
C1230 22UF 20% 6.3V X5R 805
NOSTUFF C1231 22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL NOSTUFF C1250 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1251 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1254 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1255 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1252 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1253 220UF 20% 2V POLY CASE-D2-SM1

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CPU VCORE VID CONNECTIONS

Resistors to allow for override of CPU VID
Will probably be removed before production

100 11 CPU_VID<0> — R1290 0 5% 1/16W MF-LF 402 — IMVP6_VID<0> 71 100
100 11 CPU_VID<1> — R1291 0 5% 1/16W MF-LF 402 — IMVP6_VID<1> 71 100
100 11 CPU_VID<2> — R1292 0 5% 1/16W MF-LF 402 — IMVP6_VID<2> 71 100
100 11 CPU_VID<3> — R1293 0 5% 1/16W MF-LF 402 — IMVP6_VID<3> 71 100
100 11 CPU_VID<4> — R1294 0 5% 1/16W MF-LF 402 — IMVP6_VID<4> 71 100
100 11 CPU_VID<5> — R1295 0 5% 1/16W MF-LF 402 — IMVP6_VID<5> 71 100
100 11 CPU_VID<6> — R1296 0 5% 1/16W MF-LF 402 — IMVP6_VID<6> 71 100

VCCA (CPU AVdd) DECOUPLING

11 6 =PP1V5_S0_CPU — 1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50 13 11 10 6 =PP1V05_S0_CPU — 1X 330UF, 6X 0.1UF 0402

CRITICAL C1235 330UF 20% 6.3V ELEC 6.3X8-SM
C1236 0.1UF 20% 10V CERM 402
C1237 0.1UF 20% 10V CERM 402
C1238 0.1UF 20% 10V CERM 402
C1239 0.1UF 20% 10V CERM 402
C1240 0.1UF 20% 10V CERM 402
C1241 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

Preliminary

CPU Decoupling & VID

SYNC_MASTER=MARK SYNC_DATE=10/10/2006

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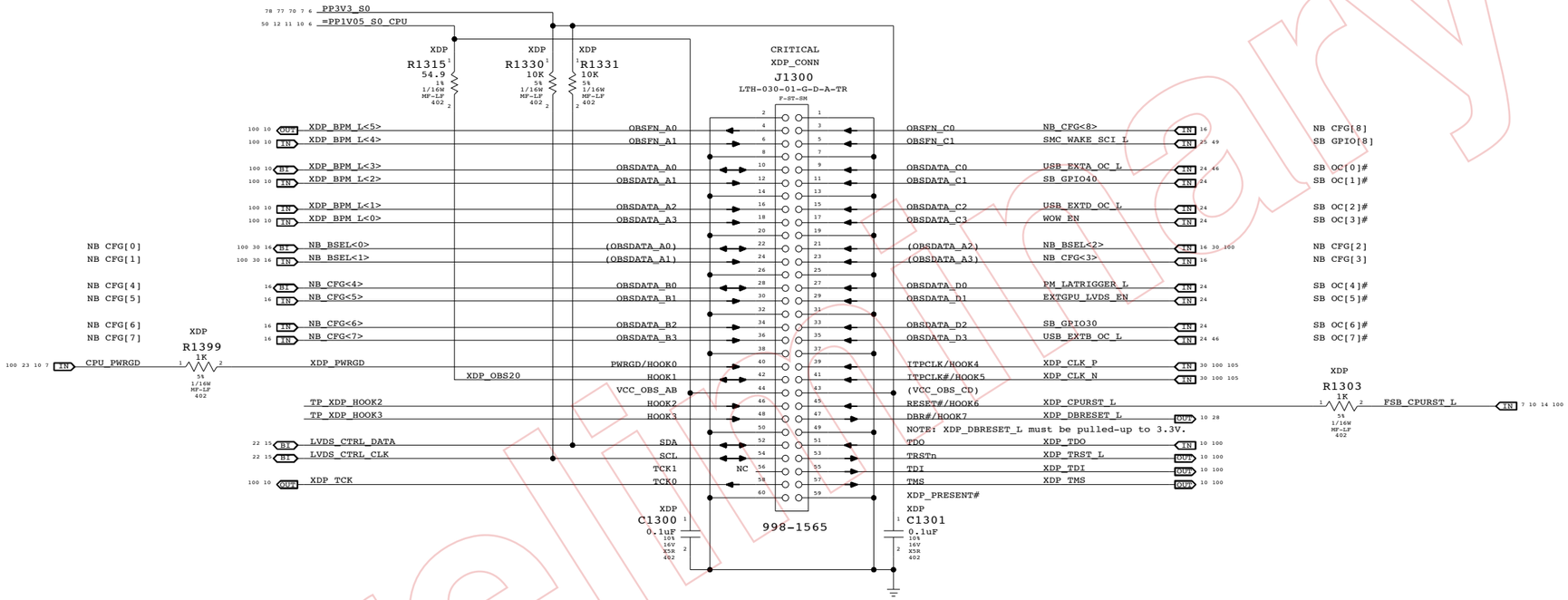
SCALE	SHT	OF
NONE	12	118

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

Preliminary

eXtended Debug Port (XDP)

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/06/2006

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D	051-7228	27
SCALE: NONE	SHT 13 OF 118	

OMIT

U1400

CRESTLINE

FCBGA

(1 OF 10)

HOST

FSB_D_L<0>	E2	H_D0*	H_A3*	J13	FSB_A_L<3>	B3	10 100
FSB_D_L<1>	G2	H_D1*	H_A4*	B11	FSB_A_L<4>	B3	10 100
FSB_D_L<2>	G1	H_D2*	H_A5*	C11	FSB_A_L<5>	B3	10 100
FSB_D_L<3>	M6	H_D3*	H_A6*	M11	FSB_A_L<6>	B3	7 10 100
FSB_D_L<4>	H1	H_D4*	H_A7*	C15	FSB_A_L<7>	B3	10 100
FSB_D_L<5>	H3	H_D5*	H_A8*	F16	FSB_A_L<8>	B3	10 100
FSB_D_L<6>	G4	H_D6*	H_A9*	L13	FSB_A_L<9>	B3	10 100
FSB_D_L<7>	F3	H_D7*	H_A10*	G17	FSB_A_L<10>	B3	10 100
FSB_D_L<8>	N8	H_D8*	H_A11*	C14	FSB_A_L<11>	B3	10 100
FSB_D_L<9>	H2	H_D9*	H_A12*	K16	FSB_A_L<12>	B3	10 100
FSB_D_L<10>	M10	H_D10*	H_A13*	B13	FSB_A_L<13>	B3	10 100
FSB_D_L<11>	N12	H_D11*	H_A14*	L16	FSB_A_L<14>	B3	10 100
FSB_D_L<12>	N9	H_D12*	H_A15*	J17	FSB_A_L<15>	B3	10 100
FSB_D_L<13>	N5	H_D13*	H_A16*	B14	FSB_A_L<16>	B3	10 100
FSB_D_L<14>	P13	H_D14*	H_A17*	K19	FSB_A_L<17>	B3	10 100
FSB_D_L<15>	K3	H_D15*	H_A18*	F15	FSB_A_L<18>	B3	10 100
FSB_D_L<16>	M2	H_D16*	H_A19*	R17	FSB_A_L<19>	B3	10 100
FSB_D_L<17>	W10	H_D17*	H_A20*	B16	FSB_A_L<20>	B3	10 100
FSB_D_L<18>	Y8	H_D18*	H_A21*	H20	FSB_A_L<21>	B3	10 100
FSB_D_L<19>	V1	H_D19*	H_A22*	L19	FSB_A_L<22>	B3	10 100
FSB_D_L<20>	N3	H_D20*	H_A23*	D17	FSB_A_L<23>	B3	10 100
FSB_D_L<21>	J1	H_D21*	H_A24*	M17	FSB_A_L<24>	B3	10 100
FSB_D_L<22>	N1	H_D22*	H_A25*	N16	FSB_A_L<25>	B3	10 100
FSB_D_L<23>	N2	H_D23*	H_A26*	J19	FSB_A_L<26>	B3	10 100
FSB_D_L<24>	M5	H_D24*	H_A27*	B18	FSB_A_L<27>	B3	7 10 100
FSB_D_L<25>	M3	H_D25*	H_A28*	E19	FSB_A_L<28>	B3	10 100
FSB_D_L<26>	M4	H_D26*	H_A29*	B17	FSB_A_L<29>	B3	10 100
FSB_D_L<27>	Y2	H_D27*	H_A30*	B15	FSB_A_L<30>	B3	10 100
FSB_D_L<28>	Y3	H_D28*	H_A31*	E17	FSB_A_L<31>	B3	10 100
FSB_D_L<29>	P4	H_D29*	H_A32*	C18	FSB_A_L<32>	B3	10 100
FSB_D_L<30>	W3	H_D30*	H_A33*	A19	FSB_A_L<33>	B3	10 100
FSB_D_L<31>	N4	H_D31*	H_A34*	B19	FSB_A_L<34>	B3	10 100
FSB_D_L<32>	AD12	H_D32*	H_A35*	N19	FSB_A_L<35>	B3	10 100
FSB_D_L<33>	AE3	H_D33*					
FSB_D_L<34>	AD9	H_D34*	H_ADS*	G12	FSB_ADS_L	B3	10 100
FSB_D_L<35>	AC9	H_D35*	H_ADSTB0*	H17	FSB_ADSTB_L<0>	B3	7 10 100
FSB_D_L<36>	AC7	H_D36*	H_ADSTB1*	G20	FSB_ADSTB_L<1>	B3	7 10 100
FSB_D_L<37>	AC14	H_D37*	H_BNR*	C8	FSB_BNR_L	B3	7 10 100
FSB_D_L<38>	AD11	H_D38*	H_BPRI*	E8	FSB_BPRI_L	OUT	10 100
FSB_D_L<39>	AC11	H_D39*	H_BREQ*	F12	FSB_BREQ0_L	B3	7 10 100
FSB_D_L<40>	AB2	H_D40*	H_DEFER*	D6	FSB_DEFER_L	OUT	10 100
FSB_D_L<41>	AD1	H_D41*	H_DBSY*	C10	FSB_DBSY_L	B3	7 10 100
FSB_D_L<42>	AB1	H_D42*	HPLL_CLK	AM5	FSB_CLK_NB_P	IN	7 30 105
FSB_D_L<43>	Y1	H_D43*	HPLL_CLK*	AM7	FSB_CLK_NB_N	IN	7 30 105
FSB_D_L<44>	AC6	H_D44*	H_DPWR*	H8	FSB_DPWR_L	B3	7 10 100
FSB_D_L<45>	AE2	H_D45*	H_DRDY*	K7	FSB_DRDY_L	B3	10 100
FSB_D_L<46>	AC3	H_D46*	H_HIT*	E4	FSB_HIT_L	B3	7 10 100
FSB_D_L<47>	AC1	H_D47*	H_HITM*	C6	FSB_HITM_L	B3	7 10 100
FSB_D_L<48>	AJ3	H_D48*	H_LOCK*	G10	FSB_LOCK_L	IN	7 10 100
FSB_D_L<49>	AH3	H_D49*	H_TRDY*	B7	FSB_TRDY_L	OUT	10 100
FSB_D_L<50>	AJ14	H_D50*					
FSB_D_L<51>	AE1	H_D51*					
FSB_D_L<52>	AE11	H_D52*					
FSB_D_L<53>	AH12	H_D53*					
FSB_D_L<54>	AJ2	H_D54*					
FSB_D_L<55>	AH5	H_D55*					
FSB_D_L<56>	AJ6	H_D56*					
FSB_D_L<57>	AE7	H_D57*					
FSB_D_L<58>	AJ7	H_D58*					
FSB_D_L<59>	AJ9	H_D59*					
FSB_D_L<60>	AE5	H_D60*					
FSB_D_L<61>	AJ4	H_D61*					
FSB_D_L<62>	AH2	H_D62*					
FSB_D_L<63>	AH13	H_D63*					

			H_DINV0*	K5	FSB_DINV_L<0>	B3	7 10 100
			H_DINV1*	L2	FSB_DINV_L<1>	B3	7 10 100
			H_DINV2*	AD13	FSB_DINV_L<2>	B3	7 10 100
			H_DINV3*	AE13	FSB_DINV_L<3>	B3	7 10 100
			H_DSTBN0*	M7	FSB_DSTB_L_N<0>	B3	7 10 100
			H_DSTBN1*	K3	FSB_DSTB_L_N<1>	B3	7 10 100
			H_DSTBN2*	AD2	FSB_DSTB_L_N<2>	B3	7 10 100
			H_DSTBN3*	AH11	FSB_DSTB_L_N<3>	B3	7 10 100
			H_DSTBP0*	L7	FSB_DSTB_L_P<0>	B3	7 10 100
			H_DSTBP1*	K2	FSB_DSTB_L_P<1>	B3	7 10 100
			H_DSTBP2*	AC2	FSB_DSTB_L_P<2>	B3	7 10 100
			H_DSTBP3*	AJ10	FSB_DSTB_L_P<3>	B3	7 10 100
			H_REQ0*	M14	FSB_REQ_L<0>	B3	7 10 100
			H_REQ1*	E13	FSB_REQ_L<1>	B3	7 10 100
			H_REQ2*	A11	FSB_REQ_L<2>	B3	7 10 100
			H_REQ3*	H13	FSB_REQ_L<3>	B3	7 10 100
			H_REQ4*	B12	FSB_REQ_L<4>	B3	7 10 100
			H_RS0*	E12	FSB_RS_L<0>	OUT	10 100
			H_RS1*	D7	FSB_RS_L<1>	OUT	10 100
			H_RS2*	D8	FSB_RS_L<2>	OUT	10 100

NB_FSB_SWING	B3	H_SWING	
NB_FSB_RCOMP	C2	H_RCOMP	
NB_FSB_SCOMP	W1	H_SCOMP	
NB_FSB_SCOMP_L	W2	H_SCOMP*	
FSB_CPURST_L	B6	H_CPURST*	100 13 10 7 OUT
FSB_CPUSLP_L	E5	H_CPUSLP*	100 10 OUT
NB_FSB_VREF	B9	H_AVREF	
	A9	H_DVREF	

30 6 =PP1V25R1V05_S0_FSB_NB

R1421 54.9 1% 1/16W MF-LF 402

R1420 54.9 1% 1/16W MF-LF 402

R1410 221 1% 1/16W MF-LF 402

R1425 1K 1% 1/16W MF-LF 402

R1426 2.0K 1% 1/16W MF-LF 402

C1425 0.1uF 10% 16V X5R 402

R1415 24.9 1% 1/16W MF-LF 402

R1411 100 1% 1/16W MF-LF 402

C1410 0.1uF 10% 16V X5R 402

Preliminary

NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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NONE	14	118

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

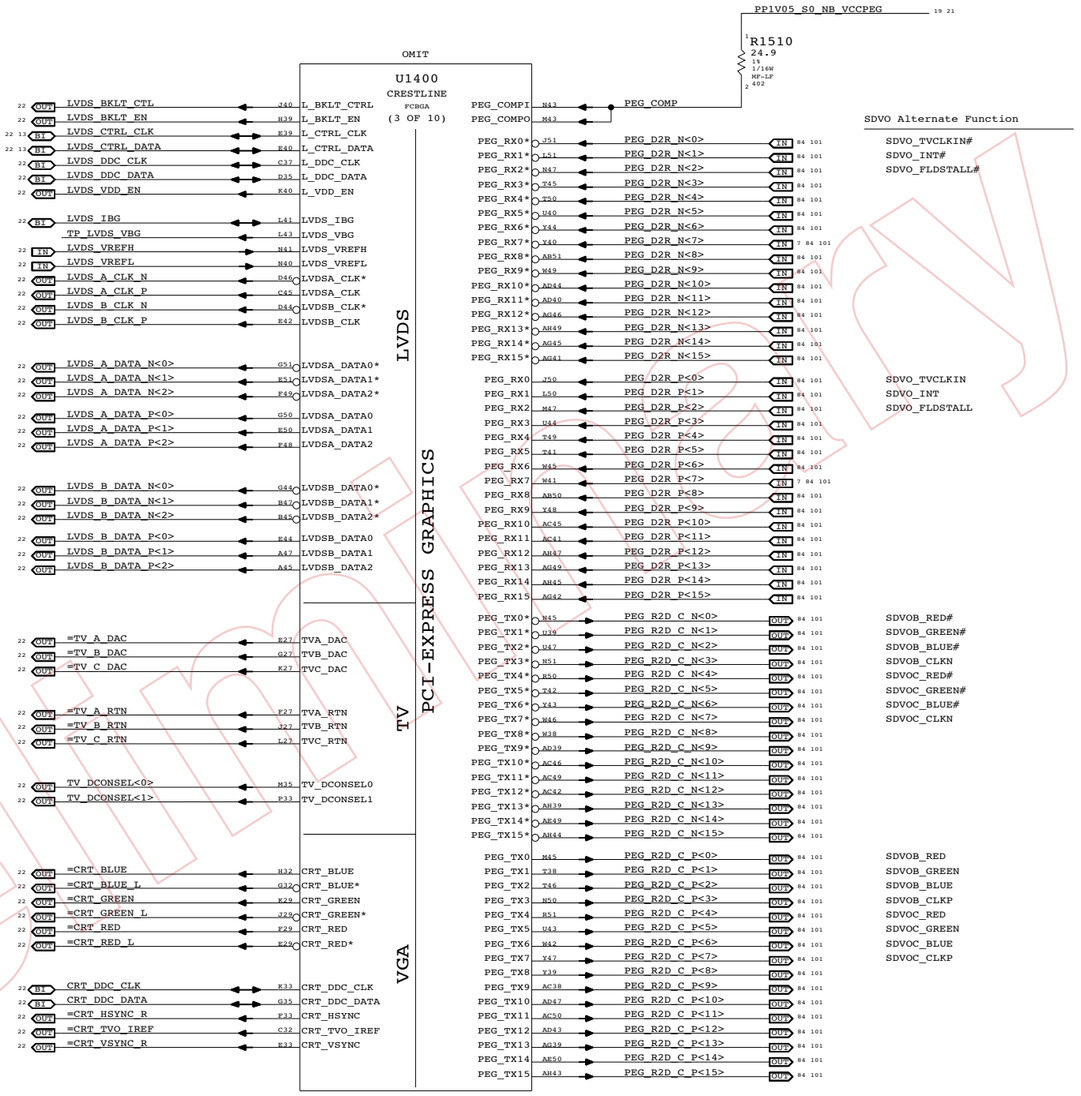
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

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Preliminary

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> — NBCFG_DMI_X2 — R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> — NBCFG_PEG_REVERSE — R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> — NBCFG_DYN_ODT_DISABLE — R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV — NBCFG_DMI_REVERSE — R1669 3.9K 5% 1/16W MF-LF 402 — NB_CFG<19>

=PP3V3_S0_NB_VCCHV — NBCFG_SDVO_AND_PCIE — R1670 3.9K 5% 1/16W MF-LF 402 — NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

=PP3V3_S0_NB_VCCHV — R1630 10K 5% 1/16W MF-LF 402 — R1631 10K 5% 1/16W MF-LF 402

PM_EXTTS_L<0>
PM_EXTTS_L<1>

OMIT

U1400 CRESTLINE FCBGA (2 OF 10)

RSVD

TP_NB_RSVD<1>	P16	RSVD1
TP_NB_RSVD<2>	P17	RSVD2
TP_NB_RSVD<3>	R35	RSVD3
TP_NB_RSVD<4>	N35	RSVD4
TP_NB_RSVD<5>	AR12	RSVD5
TP_NB_RSVD<6>	AR13	RSVD6
TP_NB_RSVD<7>	AM12	RSVD7
TP_NB_RSVD<8>	AN13	RSVD8
TP_NB_RSVD<9>	J12	RSVD9
TP_NB_RSVD<10>	AR37	RSVD10
TP_NB_RSVD<11>	AM36	RSVD11
TP_NB_RSVD<12>	AL36	RSVD12
TP_NB_RSVD<13>	AM37	RSVD13
TP_NB_RSVD<14>	D20	RSVD14
TP_NB_RSVD<20>	H10	RSVD20
TP_NB_RSVD<21>	B51	RSVD21
TP_NB_RSVD<22>	BJ20	RSVD22
TP_NB_RSVD<23>	BK22	RSVD23
TP_NB_RSVD<24>	BF19	RSVD24
TP_NB_RSVD<25>	BH20	RSVD25
TP_NB_RSVD<26>	BK18	RSVD26
TP_NB_RSVD<27>	BJ18	RSVD27
TP_MEM_CLKP2	BF23	SM_CK2
TP_MEM_CLKN2	BG23	SM_CK2*
TP_MEM_CLKP5	BC23	SM_CK5
TP_MEM_CLKN5	BD24	SM_CK5*
MEM_A_A<14>	BJ29	SA_MA14
MEM_B_A<14>	BE24	SB_MA14
TP_NB_RSVD<34>	BH39	RSVD34
TP_NB_RSVD<35>	AW20	RSVD35
TP_NB_RSVD<36>	BK20	RSVD36
TP_LVDS_A_DATAN3	C48	RSVD37
TP_LVDS_A_DATAP3	D47	RSVD38
TP_LVDS_B_DATAN3	B44	RSVD39
TP_LVDS_B_DATAP3	C44	RSVD40
TP_NB_RSVD<41>	A35	RSVD41
TP_NB_RSVD<42>	B37	RSVD42
TP_NB_RSVD<43>	B36	RSVD43
TP_NB_RSVD<44>	B34	RSVD44
TP_NB_RSVD<45>	C34	RSVD45

CFG

NB_BSEL<0>	P27	CFG0	
NB_BSEL<1>	N27	CFG1	
NB_BSEL<2>	N24	CFG2	
NB_CFG<3>	C21	CFG3	IPU
NB_CFG<4>	C23	CFG4	IPU
NB_CFG<5>	F23	CFG5	IPU
NB_CFG<6>	N21	CFG6	IPU
NB_CFG<7>	G23	CFG7	IPU
NB_CFG<8>	J20	CFG8	IPU
NB_CFG<9>	C20	CFG9	IPU
TP_NB_CFG<10>	R24	CFG10	IPU
TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	J23	CFG12	IPU
TP_NB_CFG<13>	E23	CFG13	IPU
TP_NB_CFG<14>	E20	CFG14	IPU
TP_NB_CFG<15>	K23	CFG15	IPU
NB_CFG<16>	M20	CFG16	IPU
TP_NB_CFG<17>	M24	CFG17	IPU
TP_NB_CFG<18>	L32	CFG18	IPD
NB_CFG<19>	N33	CFG19	IPD
NB_CFG<20>	L35	CFG20	IPD

PM

PM_BMBUSY_L	G41	PM_BM_BUSY*
CPU_DPRSTP_L	L33	PM_DPRSTP*
	L34	PM_EXT_TS0*
	J35	PM_EXT_TS1*
VR_PWRGOOD_DELAY	AM49	PWROK
NB_RESET_L	AV23	RSTIN*
PM_THRMTRIP_L	N23	THERMTRIP*
PM_DPRSLPVR	G36	DPRSLPVR

NC

TP_NB_NC<1>	BJ51 NC1
TP_NB_NC<2>	BK51 NC2
TP_NB_NC<3>	BK50 NC3
TP_NB_NC<4>	BL50 NC4
TP_NB_NC<5>	BL49 NC5
TP_NB_NC<6>	BL3 NC6
TP_NB_NC<7>	BL2 NC7
TP_NB_NC<8>	BK1 NC8
TP_NB_NC<9>	BJ1 NC9
TP_NB_NC<10>	B1 NC10
TP_NB_NC<11>	A5 NC11
TP_NB_NC<12>	C51 NC12
TP_NB_NC<13>	B50 NC13
TP_NB_NC<14>	A50 NC14
TP_NB_NC<15>	A49 NC15
TP_NB_NC<16>	BK2 NC16

DDR MUXING

SM_CK0	AV29	MEM_CLK_P<0>
SM_CK1	BB23	MEM_CLK_P<1>
SM_CK3	BA25	MEM_CLK_P<3>
SM_CK4	AV23	MEM_CLK_P<4>
SM_CK0*	AW30	MEM_CLK_N<0>
SM_CK1*	BA23	MEM_CLK_N<1>
SM_CK3*	AW25	MEM_CLK_N<3>
SM_CK4*	AW23	MEM_CLK_N<4>
SM_CKE0	BB29	MEM_CKE<0>
SM_CKE1	AY32	MEM_CKE<1>
SM_CKE3	BD39	MEM_CKE<3>
SM_CKE4	BG37	MEM_CKE<4>
SM_CS0*	BG20	MEM_CS_L<0>
SM_CS1*	BK16	MEM_CS_L<1>
SM_CS2*	BG16	MEM_CS_L<2>
SM_CS3*	BE13	MEM_CS_L<3>
SM_ODT0	BH18	MEM_ODT<0>
SM_ODT1	BJ15	MEM_ODT<1>
SM_ODT2	BJ14	MEM_ODT<2>
SM_ODT3	BE16	MEM_ODT<3>
SM_RCOMP	BL15	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA
SM_VREF1	AN4	=PP0V9_S3M_MEM_NBVREFB

CLK

DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N
PEG_CLK	K44	NB_CLK100M_PCIE_P
PEG_CLK*	K45	NB_CLK100M_PCIE_N

Clk used for PEG and DMI

DMI

DMI_RXN0	AN47	DMI_S2N_N<0>
DMI_RXN1	AJ38	DMI_S2N_N<1>
DMI_RXN2	AN42	DMI_S2N_N<2>
DMI_RXN3	AN46	DMI_S2N_N<3>
DMI_RXP0	AM47	DMI_S2N_P<0>
DMI_RXP1	AJ39	DMI_S2N_P<1>
DMI_RXP2	AN41	DMI_S2N_P<2>
DMI_RXP3	AN45	DMI_S2N_P<3>
DMI_TXN0	AJ46	DMI_N2S_N<0>
DMI_TXN1	AJ41	DMI_N2S_N<1>
DMI_TXN2	AM40	DMI_N2S_N<2>
DMI_TXN3	AM44	DMI_N2S_N<3>
DMI_TXP0	AJ47	DMI_N2S_P<0>
DMI_TXP1	AJ42	DMI_N2S_P<1>
DMI_TXP2	AM39	DMI_N2S_P<2>
DMI_TXP3	AM43	DMI_N2S_P<3>

GRAPHICS VID

		GFX_VID<0>
GFX_VID0	E35	GFX_VID<1>
GFX_VID1	A39	GFX_VID<2>
GFX_VID2	C38	GFX_VID<3>
GFX_VID3	B39	GFX_VID<4>
GFX_VR_EN	E36	=GFX_VR_EN

ME

CL_CLK	AM49	CLINK_NB_CLK
CL_DATA	AK50	CLINK_NB_DATA
CL_PWROK	AT43	=NB_CLINK_MPWROK
CL_RST*	AN49	CLINK_NB_RESET_L
CL_VREF	AM50	NB_CLINK_VREF

MISC

SDVO_CTRL_CLK	H35	SDVO_CTRLCLK
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA
CLKREQ*	G39	NB_CLKREQ_L
ICH_SYNC*	G40	NB_SB_SYNC_L
TEST1	A37	NB_TEST1
TEST2	R32	NB_TEST2

R1691 20K 5% 1/16W MF-LF 402 — R1690 0 5% 1/16W MF-LF 402

=PP1V8_S3M_MEM_NB

R1610 20 1% 1/16W MF-LF 402 — R1620 1K 1% 1/16W MF-LF 402 — R1622 3.01K 1% 1/16W MF-LF 402 — R1611 20 1% 1/16W MF-LF 402 — R1624 1K 1% 1/16W MF-LF 402

C1623 0.01UF 10% 16V CERM 402 — C1622 2.2UF 20% 6.3V CERM1 603 — C1625 0.01UF 10% 16V CERM 402 — C1624 2.2UF 20% 6.3V CERM1 603

C1615 0.1uF 20% 10V CERM 402 — C1616 0.1uF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD

R1640 1K 1% 1/16W MF-LF 402 — R1641 392 1% 1/16W MF-LF 402

C1640 0.1uF 20% 10V CERM 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=01/21/2007

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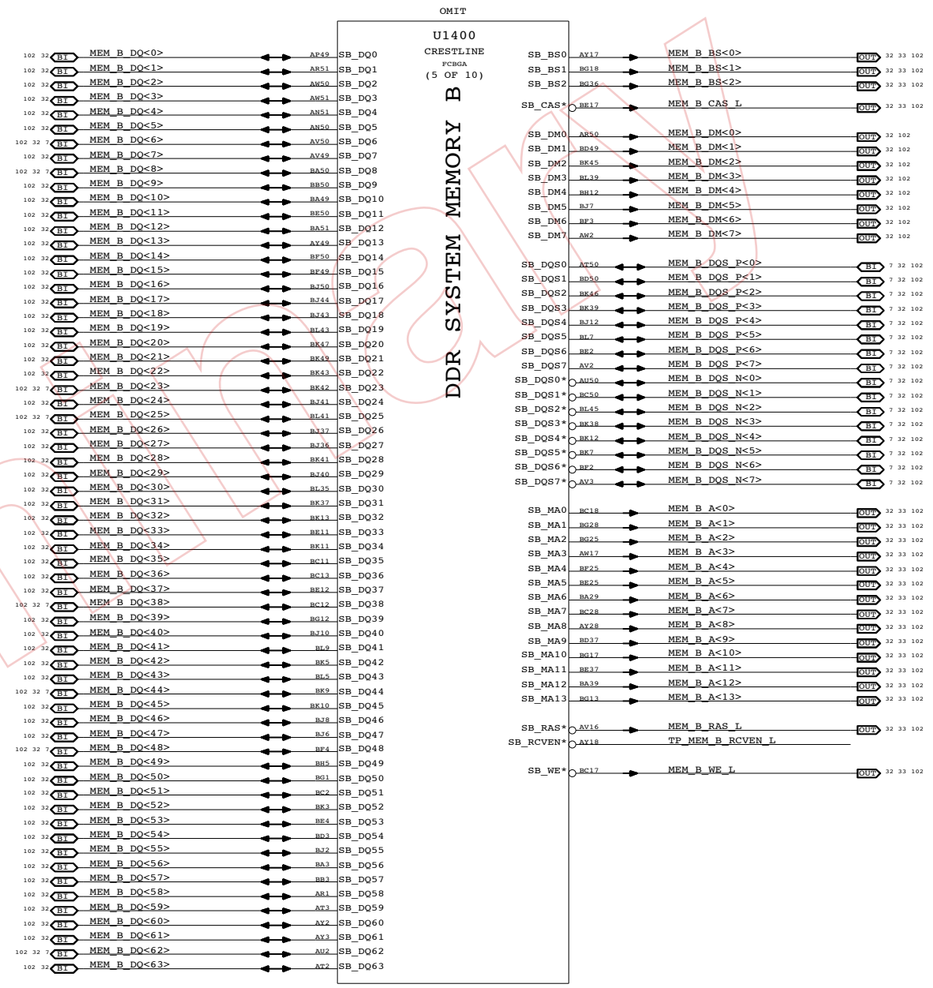
Pre-Release



Preliminary

NB DDR2 Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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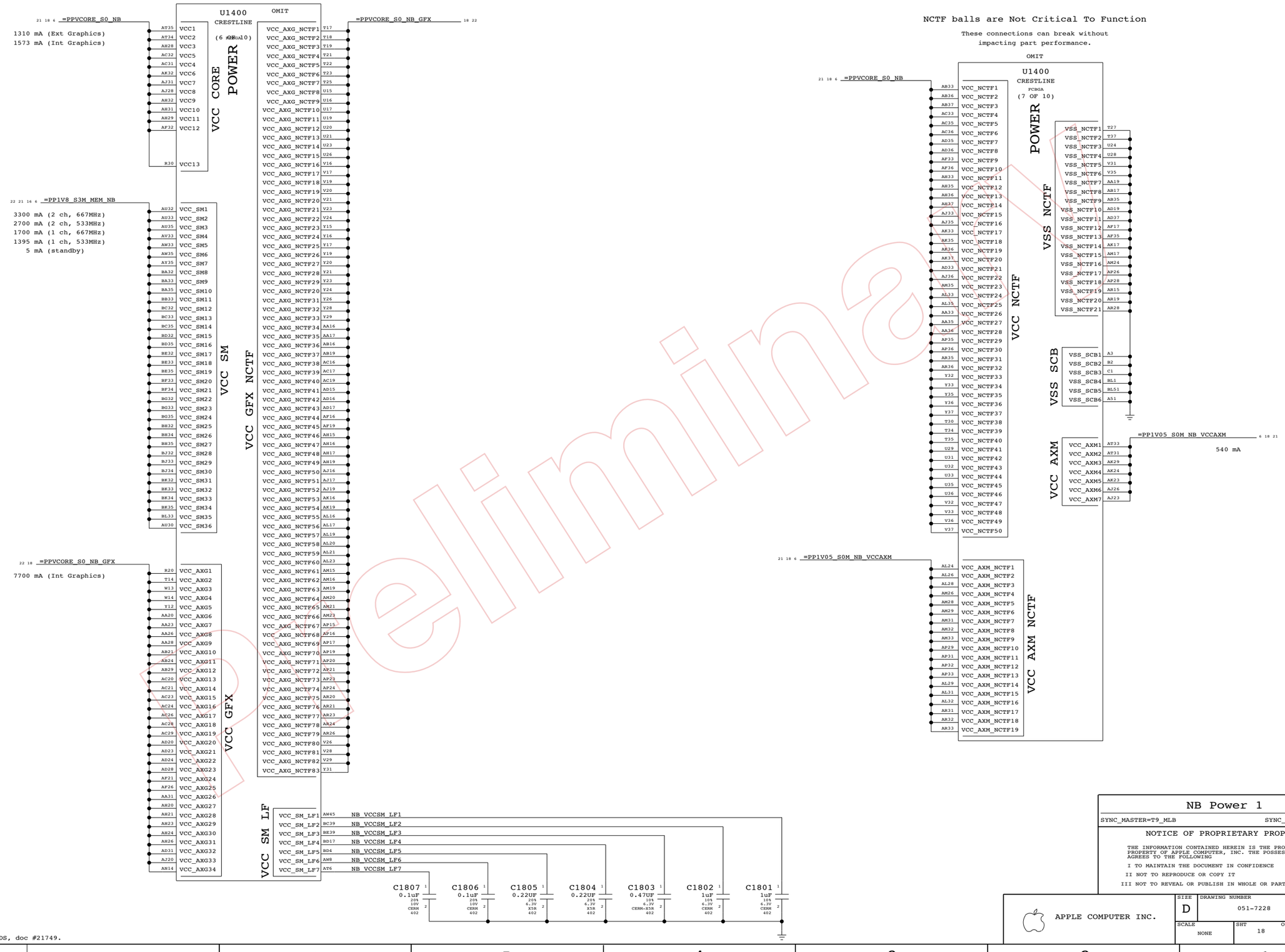
NONE	17	118



Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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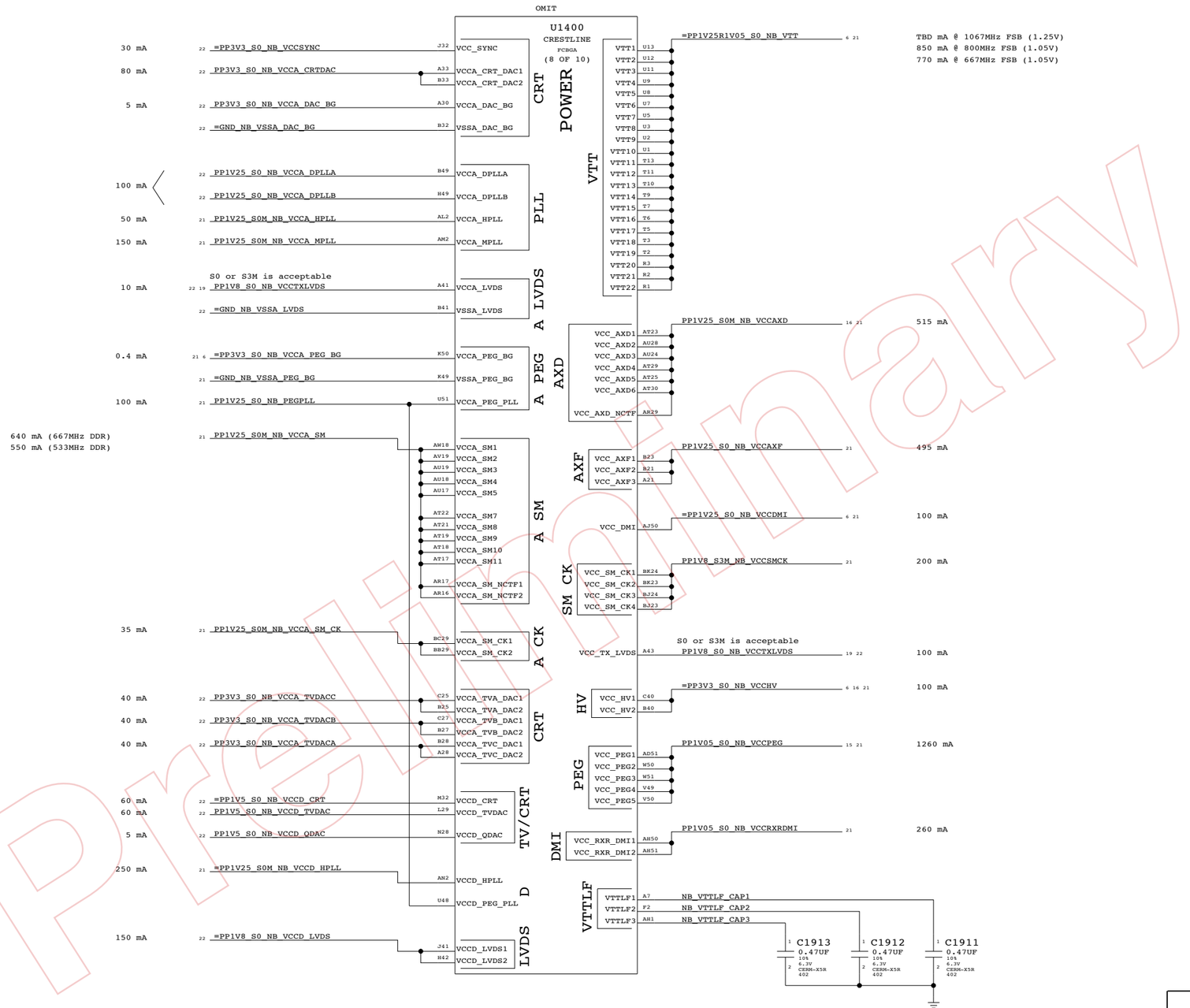
NONE	18	118



Current numbers from Crestline EDS, doc #21749.

Preliminary

NB Power 2

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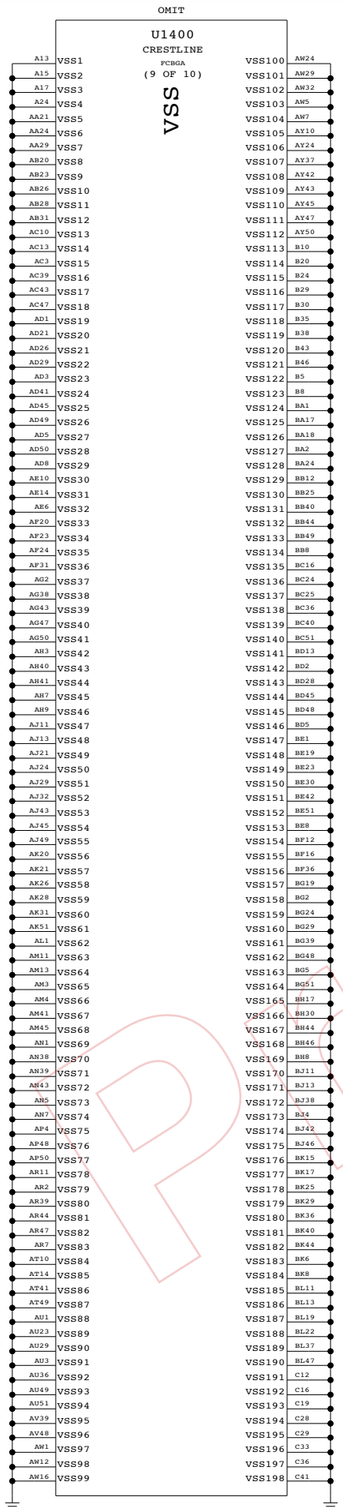
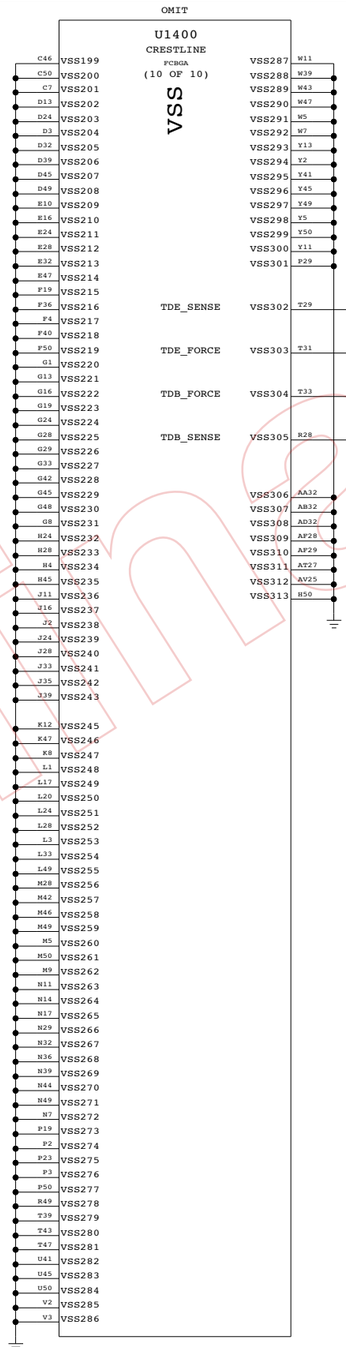
SCALE: NONE	SHT 19 OF 118	





Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

=NB_TDE_SENSE 55

NOTE: TDE = _P

=NB_TDE_FORCE 55

=NB_TDB_FORCE 55

NOTE: TDB = _N

=NB_TDB_SENSE 55

Preliminary

NB Grounds

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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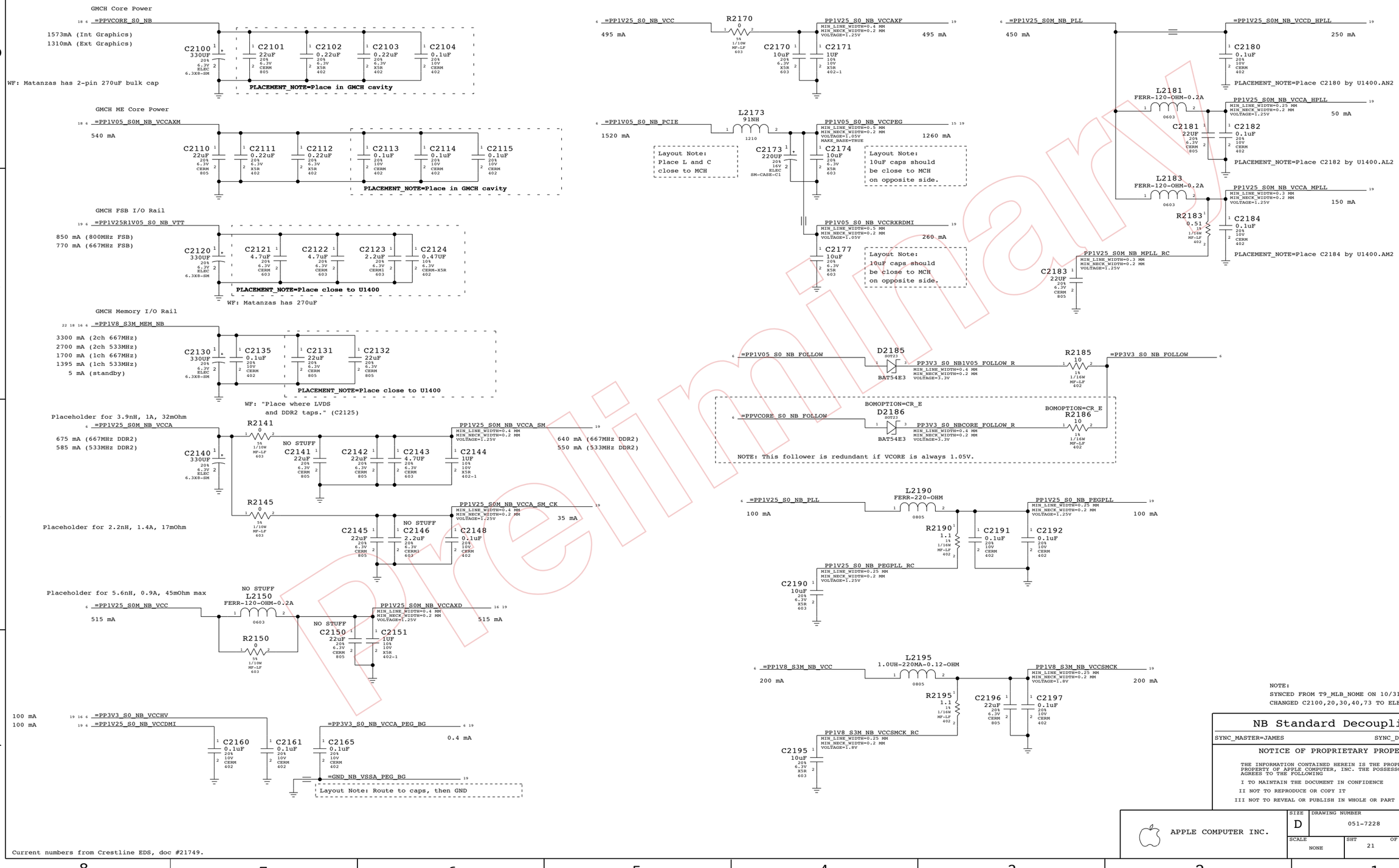
NONE	20	118


GMCH Core Power
=PPVCORE_S0_NB
1573mA (Int Graphics)
1310mA (Ext Graphics)
C2100 330UF 20% 6.3V ELEC 6.3X8-SM
C2101 22uF 20% 6.3V CERM 805
C2102 0.22uF 20% 6.3V X5R 402
C2103 0.22uF 20% 10V X5R 402
C2104 0.1uF 20% 10V CERM 402
WF: Matanzas has 2-pin 270uF bulk cap
PLACEMENT_NOTE=Place in GMCH cavity
GMCH ME Core Power
=PP1V05_S0M_NB_VCCAXM
540 mA
C2110 22uF 20% 6.3V CERM 805
C2111 0.22uF 20% 6.3V X5R 402
C2112 0.22uF 20% 6.3V X5R 402
C2113 0.1uF 20% 10V CERM 402
C2114 0.1uF 20% 10V CERM 402
C2115 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place in GMCH cavity
GMCH FSB I/O Rail
=PP1V25R1V05_S0_NB_VTT
850 mA (800MHz FSB)
770 mA (667MHz FSB)
C2120 330UF 20% 6.3V ELEC 6.3X8-SM
C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM1 603
C2124 0.47UF 10% 6.3V CERM-X5R 402
PLACEMENT_NOTE=Place close to U1400
WF: Matanzas has 270uF
GMCH Memory I/O Rail
=PP1V8_S3M_MEM_NB
3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)
C2130 330UF 20% 6.3V ELEC 6.3X8-SM
C2135 0.1uF 20% 10V CERM 402
C2131 22uF 20% 6.3V CERM 805
C2132 22uF 20% 6.3V CERM 805
PLACEMENT_NOTE=Place close to U1400
WF: "Place where LVDS and DDR2 taps." (C2125)
Placeholder for 3.9nH, 1A, 32mOhm
=PP1V25_S0M_NB_VCCA
675 mA (667MHz DDR2)
585 mA (533MHz DDR2)
R2141 0 5% 1/10W MF-LF 603
NO STUFF
C2140 330UF 20% 6.3V ELEC 6.3X8-SM
C2141 22uF 20% 6.3V CERM 805
C2142 22uF 20% 6.3V CERM 805
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402-1
PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
640 mA (667MHz DDR2)
550 mA (533MHz DDR2)
R2145 0 5% 1/10W MF-LF 603
Placeholder for 2.2nH, 1.4A, 17mOhm
NO STUFF
C2145 22uF 20% 6.3V CERM 805
C2146 2.2uF 20% 6.3V CERM1 603
C2148 0.1uF 20% 10V CERM 402
PP1V25_S0M_NB_VCCA_SM_CK
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
35 mA
Placeholder for 5.6nH, 0.9A, 45mOhm max
NO STUFF
L2150 FERR-120-OHM-0.2A 0603
=PP1V25_S0M_NB_VCC
515 mA
R2150 0 5% 1/10W MF-LF 603
NO STUFF
C2150 22uF 20% 6.3V CERM 805
C2151 1UF 10% 10V X5R 402-1
PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
515 mA
100 mA
100 mA
=PP3V3_S0_NB_VCCHV
=PP1V25_S0_NB_VCCDMI
C2160 0.1uF 20% 10V CERM 402
C2161 0.1uF 20% 10V CERM 402
=PP3V3_S0_NB_VCCA_PEG_BG
C2165 0.1uF 20% 10V CERM 402
0.4 mA
=GND_NB_VSSA_PEG_BG
Layout Note: Route to caps, then GND
Current numbers from Crestline EDS, doc #21749.
=PP1V25_S0_NB_VCC
495 mA
R2170 0 5% 1/10W MF-LF 603
C2170 10uF 20% 6.3V X5R 603
C2171 1UF 10% 10V X5R 402-1
PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
495 mA
=PP1V05_S0_NB_PCIE
1520 mA
L2173 91NH 1210
C2173 220UF 20% 16V ELEC SM-CASE-C1
Layout Note: Place L and C close to MCH
PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
1260 mA
C2174 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
260 mA
C2177 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
=PP1V25_S0M_NB_PLL
450 mA
=PP1V25_S0M_NB_VCCD_HPLL
250 mA
C2180 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2180 by U1400.AN2
L2181 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
50 mA
C2181 22UF 20% 6.3V CERM 805
C2182 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2182 by U1400.AL2
L2183 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
150 mA
R2183 0.51 1% 1/16W MF-LF 402
C2184 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2184 by U1400.AM2
PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2183 22UF 20% 6.3V CERM 805
=PP1V05_S0_NB_FOLLOW
D2185 SOT23 BAT54E3
PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
R2185 10 1% 1/16W MF-LF 402
=PP3V3_S0_NB_FOLLOW
BOMOPTION=CR_E
=PPVCORE_S0_NB_FOLLOW
D2186 SOT23 BAT54E3
PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
BOMOPTION=CR_E
R2186 10 1% 1/16W MF-LF 402
NOTE: This follower is redundant if VCORE is always 1.05V.
=PP1V25_S0_NB_PLL
100 mA
L2190 FERR-220-OHM 0805
R2190 1.1 1% 1/16W MF-LF 402
C2191 0.1uF 20% 10V CERM 402
PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
100 mA
C2192 0.1uF 20% 10V CERM 402
PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2190 10uF 20% 6.3V X5R 603
=PP1V8_S3M_NB_VCC
200 mA
L2195 1.0UH-220MA-0.12-OHM 0805
R2195 1.1 1% 1/16W MF-LF 402
C2196 22uF 20% 6.3V CERM 805
C2197 0.1uF 20% 10V CERM 402
PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
200 mA
PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
C2195 10uF 20% 6.3V X5R 603
NOTE:
SYNCED FROM T9_MLB_NOME ON 10/31/06
CHANGED C2100,20,30,40,73 TO ELEC
NB Standard Decoupling
SYNC_MASTER=JAMES
SYNC_DATE=11/03/2006
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SIZE D
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REV. 27
SCALE NONE
SHT 21 OF 118

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

15	LVDS_BKLT_CTL	TRUE	TP_LVDS_BKLT_CTL	
15	LVDS_BKLT_EN	TRUE	TP_LVDS_BKLT_EN	
15 13	LVDS_CTRL_CLK			
15 13	LVDS_CTRL_DATA			
15	LVDS_DDC_CLK			
15	LVDS_DDC_DATA			
15	LVDS_VDD_EN	TRUE	TP_LVDS_VDD_EN	
15	LVDS_IBG	TRUE	TP_LVDS_IBG	
15	LVDS_VREFH	TRUE	TP_LVDS_VREFH	
15	LVDS_VREFL	TRUE	TP_LVDS_VREFL	
15	LVDS_A_CLK_N	TRUE	TP_LVDS_A_CLK_N	
15	LVDS_A_CLK_P	TRUE	TP_LVDS_A_CLK_P	
15	LVDS_B_CLK_N	TRUE	TP_LVDS_B_CLK_N	
15	LVDS_B_CLK_P	TRUE	TP_LVDS_B_CLK_P	
15	LVDS_A_DATA_N<0>	TRUE	TP_LVDS_A_DATA_N<0>	
15	LVDS_A_DATA_N<1>	TRUE	TP_LVDS_A_DATA_N<1>	
15	LVDS_A_DATA_N<2>	TRUE	TP_LVDS_A_DATA_N<2>	
15	LVDS_A_DATA_P<0>	TRUE	TP_LVDS_A_DATA_P<0>	
15	LVDS_A_DATA_P<1>	TRUE	TP_LVDS_A_DATA_P<1>	
15	LVDS_A_DATA_P<2>	TRUE	TP_LVDS_A_DATA_P<2>	
15	LVDS_B_DATA_N<0>	TRUE	TP_LVDS_B_DATA_N<0>	
15	LVDS_B_DATA_N<1>	TRUE	TP_LVDS_B_DATA_N<1>	
15	LVDS_B_DATA_N<2>	TRUE	TP_LVDS_B_DATA_N<2>	
15	LVDS_B_DATA_P<0>	TRUE	TP_LVDS_B_DATA_P<0>	
15	LVDS_B_DATA_P<1>	TRUE	TP_LVDS_B_DATA_P<1>	
15	LVDS_B_DATA_P<2>	TRUE	TP_LVDS_B_DATA_P<2>	
15	=TV_A_DAC			
15	=TV_B_DAC			
15	=TV_C_DAC			
15	=TV_A_RTN			
15	=TV_B_RTN			
15	=TV_C_RTN			
15	TV_DCONSEL<0>			
15	TV_DCONSEL<1>			
15	=CRT_BLUE			
15	=CRT_BLUE_L			
15	=CRT_GREEN			
15	=CRT_GREEN_L			
15	=CRT_RED			
15	=CRT_RED_L			
15	CRT_DDC_CLK			
15	CRT_DDC_DATA			
15	=CRT_HSYNC_R			
15	=CRT_TVO_IREF			
15	=CRT_VSYNC_R			
16	=NB_CLK96M_DOT_P			
16	=NB_CLK96M_DOT_N			
16	=NB_CLK100M_DPLLSS_P			
16	=NB_CLK100M_DPLLSS_N			
16	SDVO_CTRLCLK			
16	SDVO_CTRLDATA			
16	GFX_VID<1>	TRUE	TP_GFX_VID<1>	
16	GFX_VID<2>	TRUE	TP_GFX_VID<2>	
16	GFX_VID<3>	TRUE	TP_GFX_VID<3>	
16	GFX_VID<4>	TRUE	TP_GFX_VID<4>	
16	=GFX_VR_EN	TRUE	TP_GFX_VR_EN	

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

	PP1V25_S0_NB_VCCA_DPLLA		19
	PP1V25_S0_NB_VCCA_DPLLB		19
	=PP1V5_S0_NB_VCCD_CRT		19
	PP1V5_S0_NB_VCCD_QDAC		19
	=PPVCORE_S0_NB_GFX		18
	PP3V3_S0_NB_VCCA_CRTDAC		19
	PP3V3_S0_NB_VCCA_TVDACA		19
	PP3V3_S0_NB_VCCA_TVDACB		19
	PP3V3_S0_NB_VCCA_TVDACC		19
	PP3V3_S0_NB_VCCA_DAC_BG		19
	=GND_NB_VSSA_DAC_BG		19
	PP1V8_S0_NB_VCCTXLVDS		19
TP_NB_VSSA_LVDS	=GND_NB_VSSA_LVDS		19
	=PP1V8_S0_NB_VCCD_LVDS		19
	=PP3V3_S0_NB_VCCSYNC		19

NOTE:
SANTA ROSA PLATFORM P180 FIG 119 - NC
ALSO CONFIRMED WITH INTEL

16	=NB_CLINK_MPWROK	TRUE	VR_PWRGOOD_DELAY	7 16 70 71

VCCD_TVDAC ALSO POWERS INTERNAL THERMAL SENSORS.

6 =PP1V5_S0_NB_TVDAC — 65 mA

C2213 10uF 20% 6.3V X5R 603

C2200 0.1uF 20% 10V CERM 402

C2201 22000pF-1000mA 16V NPN18

PP1V5_S0_NB_VCCD_TVDAC 19 — 60 mA
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V

Layout Note:
THESE CAPS SHOULD BE
within 6.35 mm of NB edge

21 18 16 6 =PP1V8_S3M_MEM_NB

R2200 1K 5% 1/16W MF-LF 402

R2202 1K 5% 1/16W MF-LF 402

R2201 1K 5% 1/16W MF-LF 402

R2203 1K 5% 1/16W MF-LF 402

PP0V9_S3M_MEM_NBVREFA	TRUE	=PP0V9_S3M_MEM_NBVREFA	7 16
VOLTAGE=0.9V MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.25MM			
PP0V9_S3M_MEM_NBVREFB	TRUE	=PP0V9_S3M_MEM_NBVREFB	7 16
VOLTAGE=0.9V MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.25MM			

Preliminary

NB Graphics Decoupling

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

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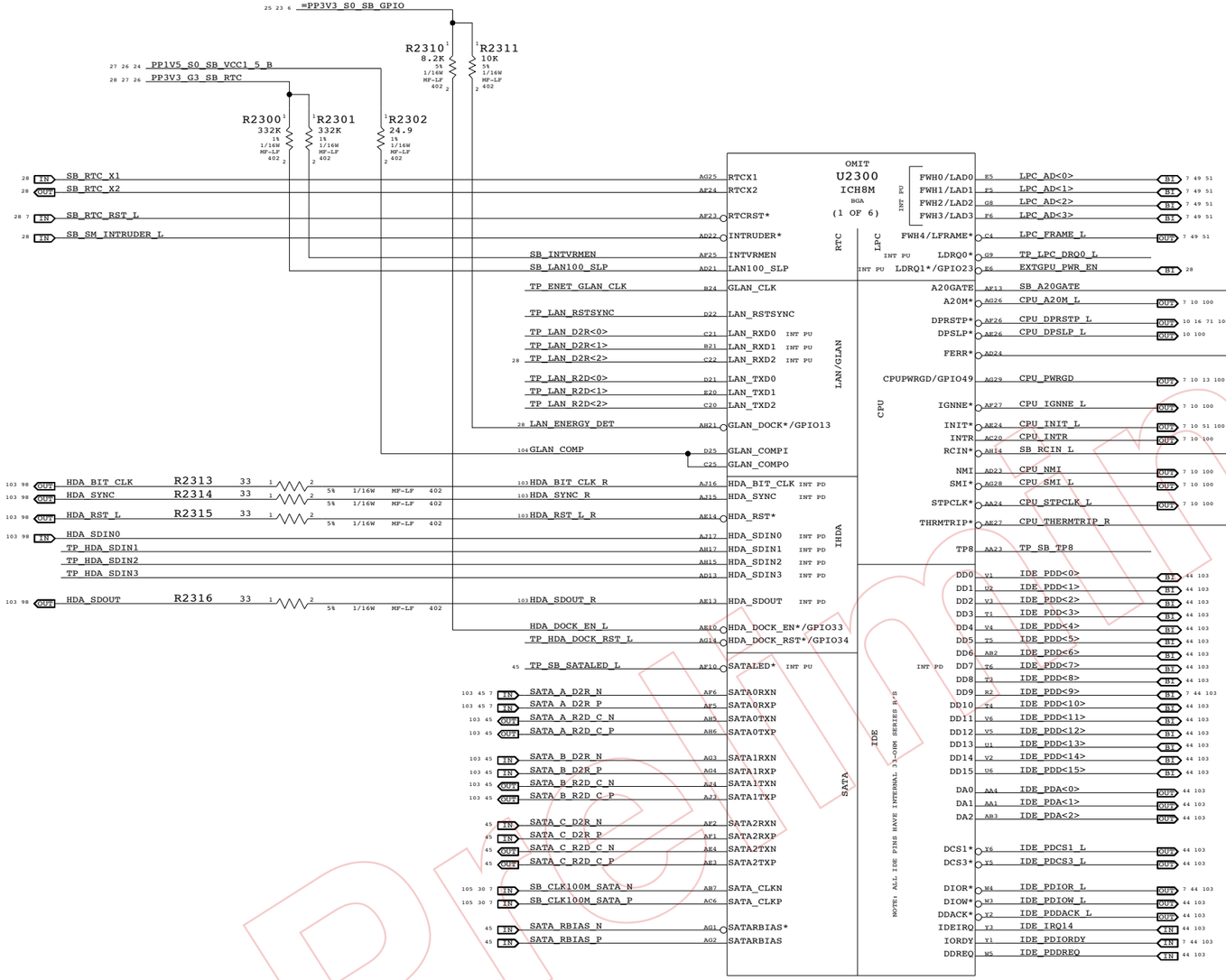

	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=03/22/2007

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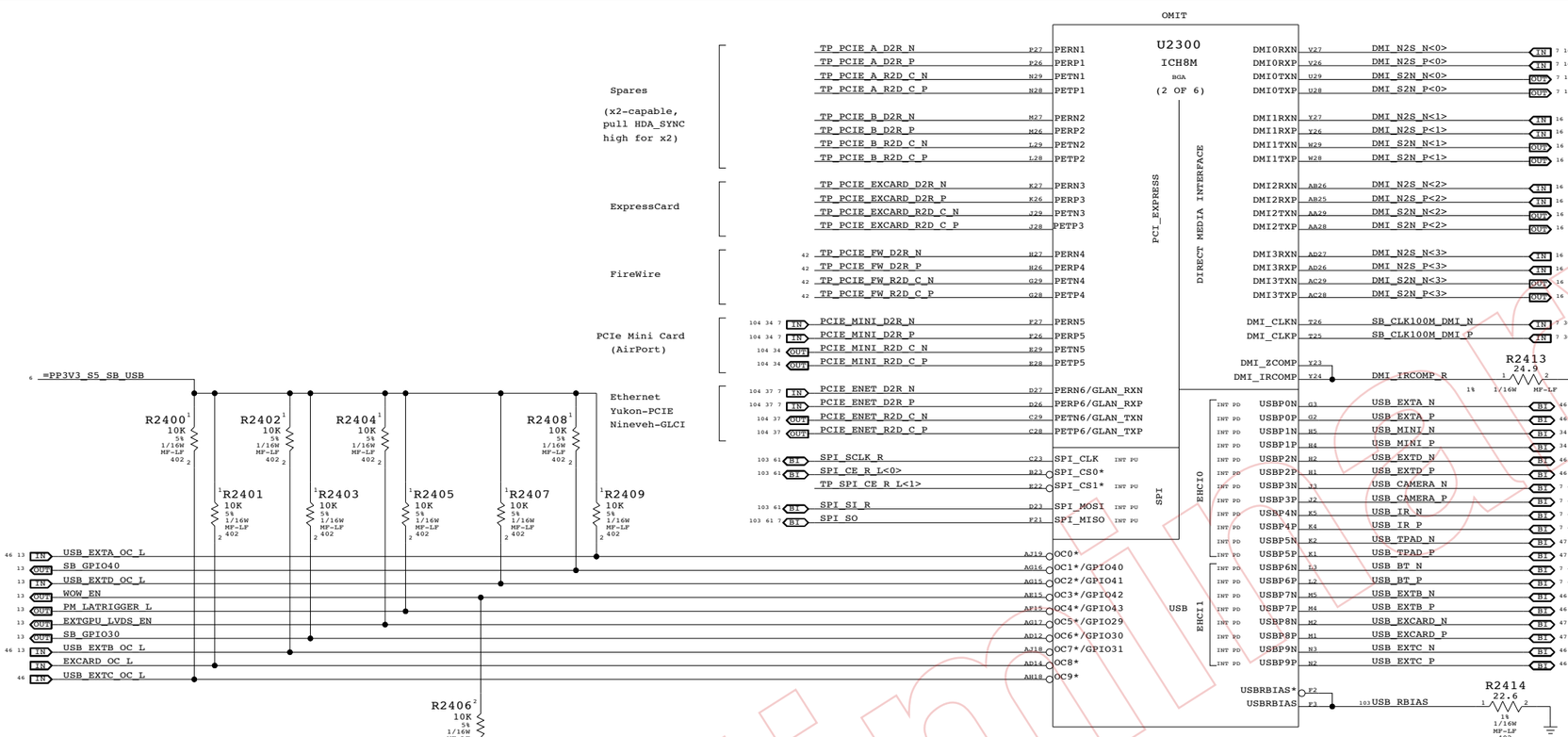
OMIT
U2300
ICH8M
BGA
(2 OF 6)
PCI_EXPRESS
DIRECT MEDIA INTERFACE
SPI
USB
EHCI1
EHCI0
Spares
(x2-capable, pull HDA_SYNC high for x2)
ExpressCard
FireWire
PCIe Mini Card (AirPort)
Ethernet Yukon-PCIE Nineveh-GLCI
TP_PCIE_A_D2R_N
TP_PCIE_A_D2R_P
TP_PCIE_A_R2D_C_N
TP_PCIE_A_R2D_C_P
TP_PCIE_B_D2R_N
TP_PCIE_B_D2R_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_R2D_C_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_FW_D2R_N
TP_PCIE_FW_D2R_P
TP_PCIE_FW_R2D_C_N
TP_PCIE_FW_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
SPI_SCLK_R
SPI_CE_R_L<0>
TP_SPI_CE_R_L<1>
SPI_SI_R
SPI_SO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI
SPI_MISO
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_IRCOMP_R
R2413
24.9
PP1V5_S0_SB_VCC1_5_B
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USB_EXTA_N
USB_EXTA_P
USB_MINI_N
USB_MINI_P
USB_EXTD_N
USB_EXTD_P
USB_CAMERA_N
USB_CAMERA_P
USB_IR_N
USB_IR_P
USB_TPAD_N
USB_TPAD_P
USB_BT_N
USB_BT_P
USB_EXTB_N
USB_EXTB_P
USB_EXCARD_N
USB_EXCARD_P
USB_EXTC_N
USB_EXTC_P
External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Geyser Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C
NOTE: USBP[0-9]P/N have internal 15K pull-downs.
USBRBIAS*
USBRBIAS
R2414
22.6
USB_RBIAS
=PP3V3_S5_SB_USB
R2400
R2401
R2402
R2403
R2404
R2405
R2407
R2408
R2409
10K
USB_EXTA_OC_L
SB_GPIO40
USB_EXTD_OC_L
WOW_EN
PM_LATRIGGER_L
EXTGPU_LVDS_EN
SB_GPIO30
USB_EXTB_OC_L
EXCARD_OC_L
USB_EXTC_OC_L
OC0*
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
OC8*
OC9*
R2406
10K
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.
PCI
INTERRUPT I/F
REQ0*
GNT0*
REQ1*/GPIO50
GNT1*/GPIO51
REQ2*/GPIO52
GNT2*/GPIO53
REQ3*/GPIO54
GNT3*/GPIO55
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCIRST*
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
FRAME*
PLTRST*
PCICLK
PME*
PCI_FW_REQ_L
PCI_REQ1_L
TP_SB_GPIO51
PCI_REQ2_L
TP_SB_GPIO53
ODD_RST_5VTOL_L
TP_SB_GPIO55
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_RST_L
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PCI_FRAME_L
PLT_RST_L
PCI_CLK33M_SB
TP_PCI_PME_L
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
FireWire INT*
PIRQE*/GPIO2
PIRQF*/GPIO3
PIRQG*/GPIO4
PIRQH*/GPIO5
INT_PIRQE_L
INT_PIRQF_L
DVI_HOTPLUG_DET
ODD_PWR_EN_L
Provide a pull-down on this GPIO if not used.
PCI_FW_GNT_L
BOOT_LPC_SPI_L
MAKE_BASE=TRUE
R2415
1K
R2415 pull-down on GNT0# selects SPI ROM by default.
SB BOOT BIOS SELECT
I/F
GNT0#
LPC
1
SPI
0
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
=PP3V3_S0_SB_PCI
R2423
R2424
R2425
R2426
R2427
R2428
R2430
R2429
R2432
R2431
R2433
R2437
R2436
R2438
R2439
R2440
R2441
R2442
8.2K
SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_MLB_NOME
SYNC_DATE=03/22/2007
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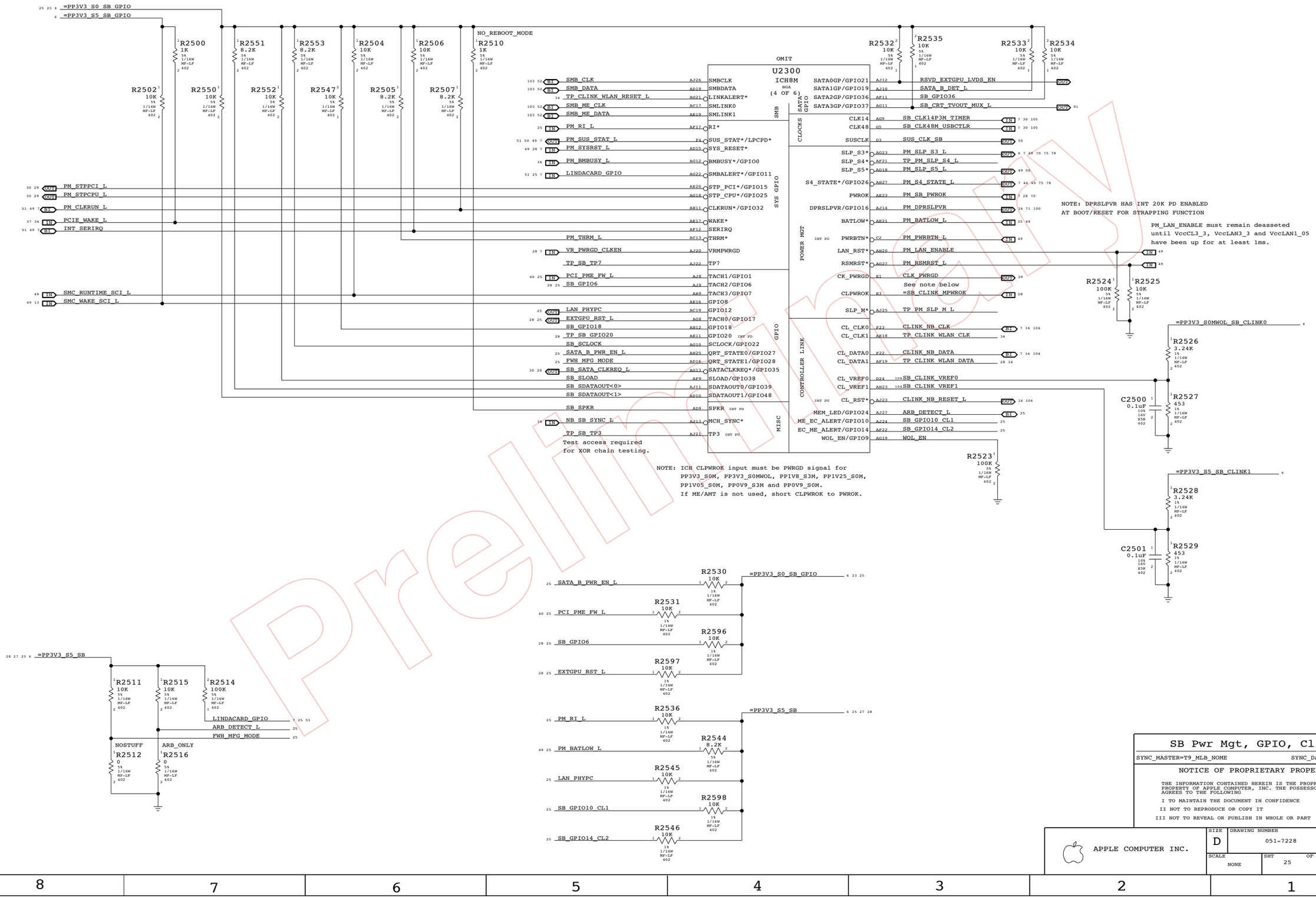
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-7228
REV.
27
SCALE
NONE
SHT
24
OF
118



Preliminary

SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=03/22/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 25 OF 118	

Preliminary

U2300
ICH8M
BGA
(5 OF 6)
OMIT

VSS
VSS_NCTF

U2300
ICH8M
BGA
(6 OF 6)
OMIT

6 uA S0-G3	28 27 23	PP3V3_G3_SB_RTC	AD25	VCCRTC		
1 mA	27	PP5V_S0_SB_V5REF	A16	V5REF		
			T7			
1 mA S0-S5	27	PP5V_S5_SB_V5REF_SUS	G4	V5REF_SUS		
657 mA	27 24 23	PP1V5_S0_SB_VCC1_5_B	AA25	VCC1_5_B	VCCA3GP	
			AA26			
			AA27			
			AB27			
			AB28			
			AB29			
			D28			
			D29			
			E25			
			E26			
			E27			
			F24			
			F25			
			G24			
			H23			
			H24			
			J23			
			J24			
			K24			
			K25			
			L23			
			L24			
			L25			
			M24			
			M25			
			N23			
			N24			
			N25			
			P24			
			P25			
			R24			
			R25			
			R26			
			R27			
			T23			
			T24			
			T27			
			T28			
			T29			
			U24			
			W25			
			V24			
			U25			
			Y25			
			V25			
			V23			
47 mA	27	PP1V5_S0_SB_VCCSATAPLL	AJ6	VCCSATAPLL		
1080 mA (VCC1_5_A total)	27 6	=PP1V5_S0_SB_VCC1_5_A_ARX	AE7	VCC1_5_A	ARX	
			AF7			
			AG7			
			AH7			
			AJ7			
	27 6	=PP1V5_S0_SB_VCC1_5_A_ATX	AC1	VCC1_5_A	ATX	
			AC2			
			AC3			
			AC4			
			AC5			
	6	=PP1V5_S0_SB_VCC1_5_A	AC10	VCC1_5_A		
			AC9			
			AA5	VCC1_5_A		
			AA6			
			G12	VCC1_5_A		
			G17			
	27 6	=PP1V5_S0_SB_VCC1_5_A_USB_CORE	H7			
			AC7	VCC1_5_A		
			AD7			
10 mA	27 6	=PP1V5_S0_SB_VCCUSBPLL	D1	VCCUSBPLL		
			F1	VCC1_5_A	USB CORE	
			L6			
			L7			
			M6			
			M7			
			W23	VCC1_5_A24		
		TP_VCCLAN1_05_INTERNAL_REG1	F17	VCCLAN1_05		
		TP_VCCLAN1_05_INTERNAL_REG2	G18			
19 mA S0, 63 mA M1 & WOL	27 6	=PP3V3_S0MWOL_SB_VCCCL3_3	F20	VCCCL3_3		
			G21			
23 mA	27	PP1V5_S0_SB_VCCGLANPLL	A24	VCCGLANPLL	GLAN POWER	
80 mA	27	=PP1V5_S0_SB_VCCGLAN1_5	B27	VCCGLAN1_5		
			A27			
			B28			
			B26			
			A26			
1 mA	6	=PP3V3_S0_SB_VCCGLAN3_3	B25	VCCGLAN3_3		

		=PPVCORE_S0_SB	A13	6 27	1130 mA	
			B13			
			C13			
			D14			
			E14			
			F14			
			G14			
			I11			
			I12			
			I14			
			I16			
VCC1_05			I17			CORE
			I18			
			M11			
			M18			
			P11			
			P18			
			T11			
			T18			
			U18			
			V17			
			V14			
			V11			
			U11			
			V18			
			V16			
			V12			
VCCDMIPLL		PP1V5_S0_SB_VCCDMIPLL	R29	27	23 mA	
		=PP1V25_S0_SB_DMI	AE28	6 27	50 mA	
VCC_DMI			AE29			
		=PP1V05_S0_SB_CPU_IO	AC23	6 23 27	1 mA	
V_CPU_IO			AC24			
VCC3_3		=PP3V3_S0_SB_VCC3_3_DMI	AF29	6 27		
VCC3_3		=PP3V3_S0_SB_VCC3_3_SATA	AD2	6 27		
		=PP3V3_S0_SB_VCC3_3_VCCPCORE	AC8	6		
VCC3_3			AD8			VCCP CORE
			AE8			
			AF8			
		=PP3V3_S0_SB_VCC3_3_IDE	AA3	6 27	442 mA	
			U7		(VCC3_3 total)	
VCC3_3			V7			IDE
			W1			
			W6			
			W7			
			Y7			
		=PP3V3_S0_SB_VCC3_3_PCI	A8	6 27		
			B15			
			B18			
			B4			
			B9			
VCC3_3			C15			PCI
			D13			
			D5			
			E10			
			E7			
			F11			
VCCHDA		=PP3V3R1V5_S0_SB_VCCHDA	AC12	6 27	32 mA	
VCCSUSHDA		=PP3V3_S5_SB_3V3_VCCSUSHDA	AD11	6 27	11 mA S0, 1 mA S3-S5	
VCCSUS1_05		TP_VCCSUS1_05_INTERNAL_REG1	J6			
		TP_VCCSUS1_05_INTERNAL_REG2	AF20			
VCCSUS1_5		TP_VCCSUS1_5_INTERNAL_REG1	AC16			
VCCSUS1_5		TP_VCCSUS1_5_INTERNAL_REG2	J7			
VCCSUS3_3		=PP3V3_S5_SB_VCCSUS3_3	C3	6 27		
			AC18			
			AC21			
VCCSUS3_3			AC22			VCCPSUS
			AG29			
			AH28			
		=PP3V3_S5_SB_VCCSUS3_3_USB	P6	6 27	117 mA S0, 44 mA S3-S5	
			P7		(VCCSUS3_3 total)	
			C1			
			N7			
			P1			
VCCSUS3_3			P2			VCCPUSB
			P3			
			P4			
			P5			
			R1			
			R3			
			R5			
			R6			
VCCCL1_05		TP_VCCCL1_05_INTERNAL_REG	G22			
VCCCL1_5		VCCCL1_5V	A22			
VCCLAN3_3		=PP3V3_S0MWOL_SB_VCCLAN3_3	F19	6 27	19 mA S0, 51 mA M1 & WOL	
			G20			

C2600 1uF 10% 6.3V CERM 402
C2601 0.1uF 20% 10V CERM 402

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.

Current figures provided assume 1.5V.

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Power & Ground

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=03/22/2007

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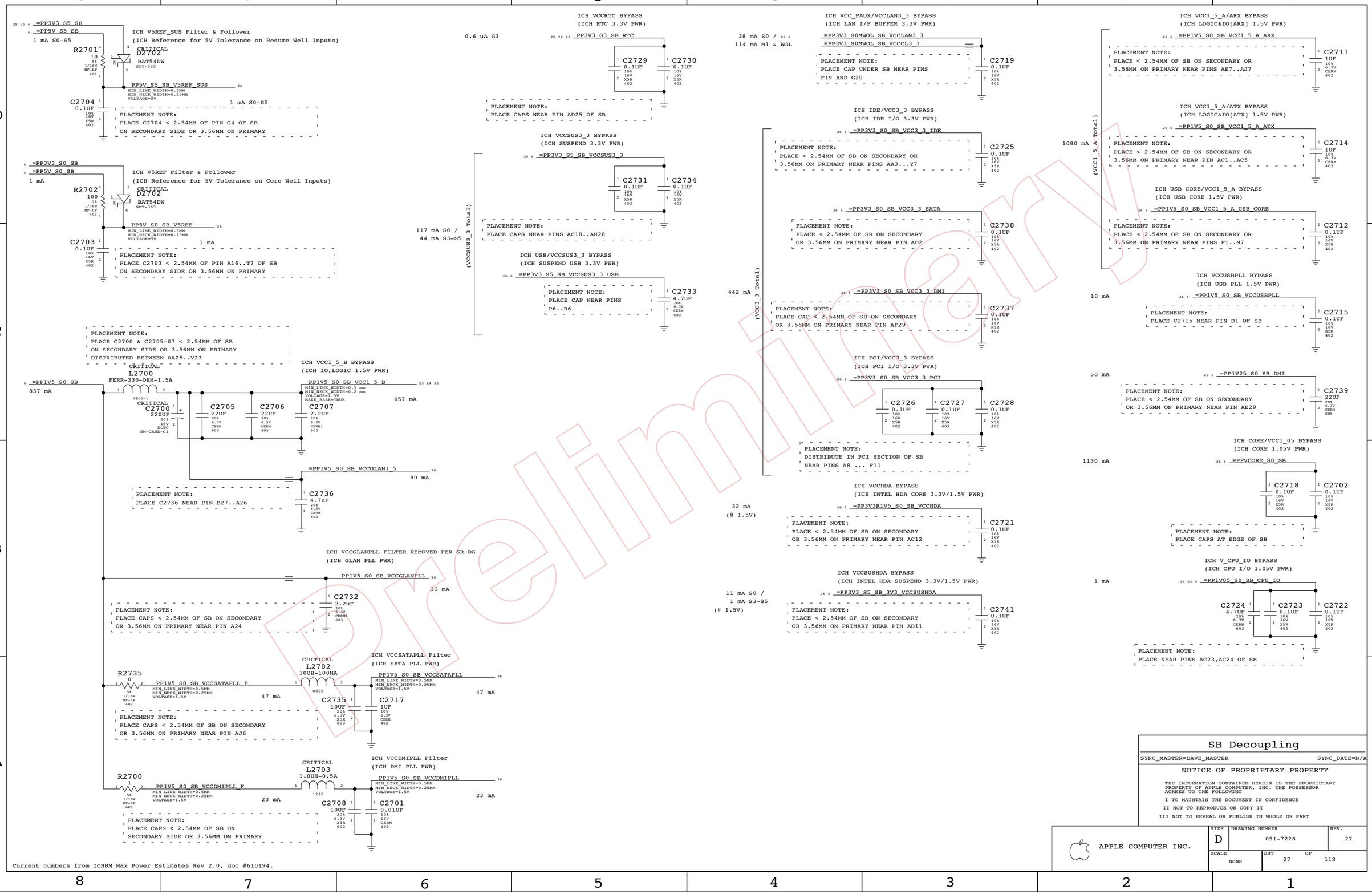
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE	SHT	OF
NONE	26	118


ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5
R2701 10 5% 1/16W MF-LF 402
CRITICAL
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
=PP3V3_S0_SB
=PP5V_S0_SB
1 mA
R2702 100 5% 1/16W MF-LF 402
CRITICAL
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 0.1UF 10% 16V X5R 402
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23
ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
=PP1V5_S0_SB
837 mA
CRITICAL
L2700 FERR-330-OHM-1.5A 0805-1
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA
CRITICAL
C2700 220UF 20% 16V ELEC SM-CASE-C1
C2705 22UF 20% 6.3V CERM 805
C2706 22UF 20% 6.3V CERM 805
C2707 2.2UF 20% 6.3V CERM1 603
=PP1V5_S0_SB_VCCGLAN1_5
80 mA
C2736 4.7uF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26
ICH VCCGLANPLL FILTER REMOVED PER SR DG
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
C2732 2.2uF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24
ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/16W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
CRITICAL
L2702 10UH-100MA 0805
C2735 10UF 20% 6.3V X5R 603
PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
C2717 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6
ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
CRITICAL
L2703 1.0UH-0.5A 1210
C2708 10UF 20% 6.3V X5R 603
PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
C2701 0.01UF 10% 16V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28
117 mA S0 /
44 mA S3-S5
(VCCSUS3_3 Total)
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
C2733 4.7uF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3
C2719 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
C2725 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7
=PP3V3_S0_SB_VCC3_3_SATA
C2738 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2
442 mA
(VCC3_3 Total)
=PP3V3_S0_SB_VCC3_3_DMI
C2737 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11
ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
C2721 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12
ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
C2741 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2711 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
1080 mA
(VCC1_5_A Total)
C2714 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
C2712 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
C2715 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB
50 mA
=PP1V25_S0_SB_DMI
C2739 22UF 20% 6.3V CERM 805
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Decoupling
SYNC_MASTER=DAVE_MASTER
SYNC_DATE=N/A
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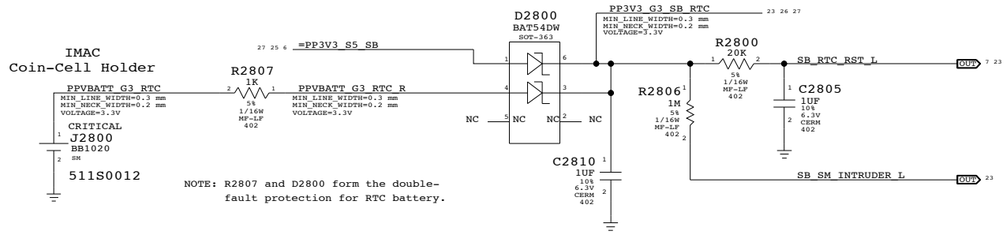
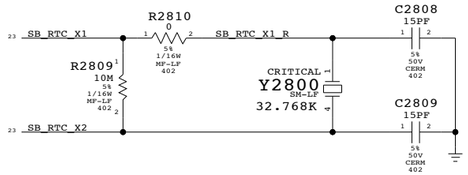
SIZE D
DRAWING NUMBER 051-7228
REV. 27
SCALE NONE
SHT 27 OF 118
Preliminary

RTC Power Sources



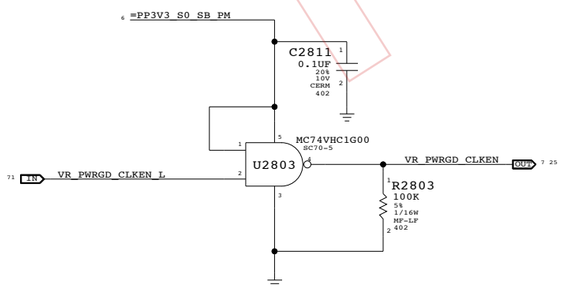
SB RTC Crystal



CPU VCORE FORCEPSI UNUSED

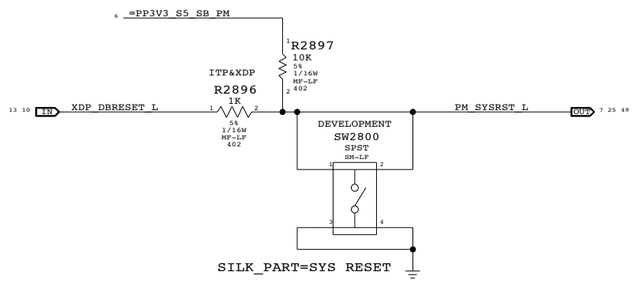
PWROK = CLINK PWROK FOR NO ME

VRMPWRGD INVERTER



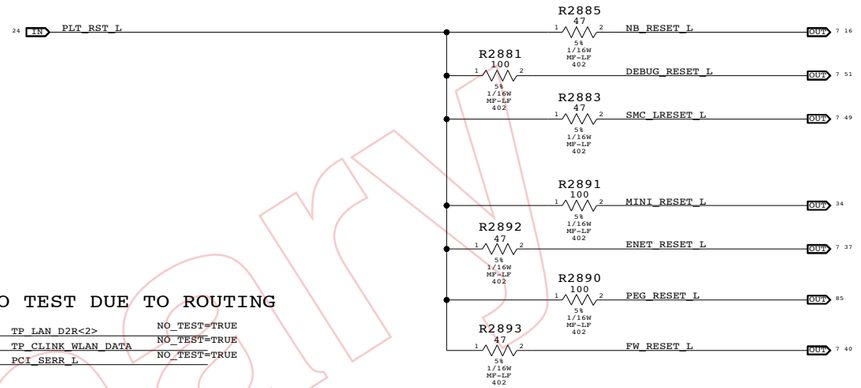
UNUSED PCI BUS

PCI_AD<0>	MAKE_BASE=TRUE	TP_PCI_AD_0
PCI_AD<1>	MAKE_BASE=TRUE	TP_PCI_AD_1
PCI_AD<2>	MAKE_BASE=TRUE	TP_PCI_AD_2
PCI_AD<3>	MAKE_BASE=TRUE	TP_PCI_AD_3
PCI_AD<4>	MAKE_BASE=TRUE	TP_PCI_AD_4 NO_TEST=TRUE
PCI_AD<5>	MAKE_BASE=TRUE	TP_PCI_AD_5
PCI_AD<6>	MAKE_BASE=TRUE	TP_PCI_AD_6
PCI_AD<7>	MAKE_BASE=TRUE	TP_PCI_AD_7
PCI_AD<8>	MAKE_BASE=TRUE	TP_PCI_AD_8
PCI_AD<9>	MAKE_BASE=TRUE	TP_PCI_AD_9
PCI_AD<10>	MAKE_BASE=TRUE	TP_PCI_AD_10
PCI_AD<11>	MAKE_BASE=TRUE	TP_PCI_AD_11
PCI_AD<12>	MAKE_BASE=TRUE	TP_PCI_AD_12
PCI_AD<13>	MAKE_BASE=TRUE	TP_PCI_AD_13
PCI_AD<14>	MAKE_BASE=TRUE	TP_PCI_AD_14
PCI_AD<15>	MAKE_BASE=TRUE	TP_PCI_AD_15
PCI_AD<16>	MAKE_BASE=TRUE	TP_PCI_AD_16
PCI_AD<17>	MAKE_BASE=TRUE	TP_PCI_AD_17
PCI_AD<18>	MAKE_BASE=TRUE	TP_PCI_AD_18
PCI_AD<19>	MAKE_BASE=TRUE	TP_PCI_AD_19
PCI_AD<20>	MAKE_BASE=TRUE	TP_PCI_AD_20
PCI_AD<21>	MAKE_BASE=TRUE	TP_PCI_AD_21
PCI_AD<22>	MAKE_BASE=TRUE	TP_PCI_AD_22
PCI_AD<23>	MAKE_BASE=TRUE	TP_PCI_AD_23
PCI_AD<24>	MAKE_BASE=TRUE	TP_PCI_AD_24
PCI_AD<25>	MAKE_BASE=TRUE	TP_PCI_AD_25
PCI_AD<26>	MAKE_BASE=TRUE	TP_PCI_AD_26
PCI_AD<27>	MAKE_BASE=TRUE	TP_PCI_AD_27
PCI_AD<28>	MAKE_BASE=TRUE	TP_PCI_AD_28
PCI_AD<29>	MAKE_BASE=TRUE	TP_PCI_AD_29
PCI_AD<30>	MAKE_BASE=TRUE	TP_PCI_AD_30
PCI_AD<31>	MAKE_BASE=TRUE	TP_PCI_AD_31
PCI_C_BE_L<0>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_0
PCI_C_BE_L<1>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_1
PCI_C_BE_L<2>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_2
PCI_C_BE_L<3>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_3
PCI_RST_L	MAKE_BASE=TRUE	TP_PCI_RST_L
PCI_PAR	MAKE_BASE=TRUE	TP_PCI_PAR

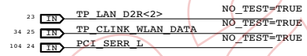


Platform Reset Connections

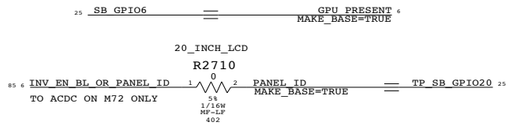
Unbuffered



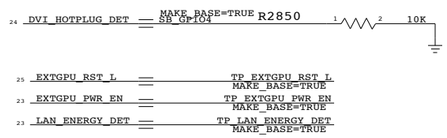
NO TEST DUE TO ROUTING



RE-PURPOSED GPIOS



UNUSED GPIOS



SB Misc

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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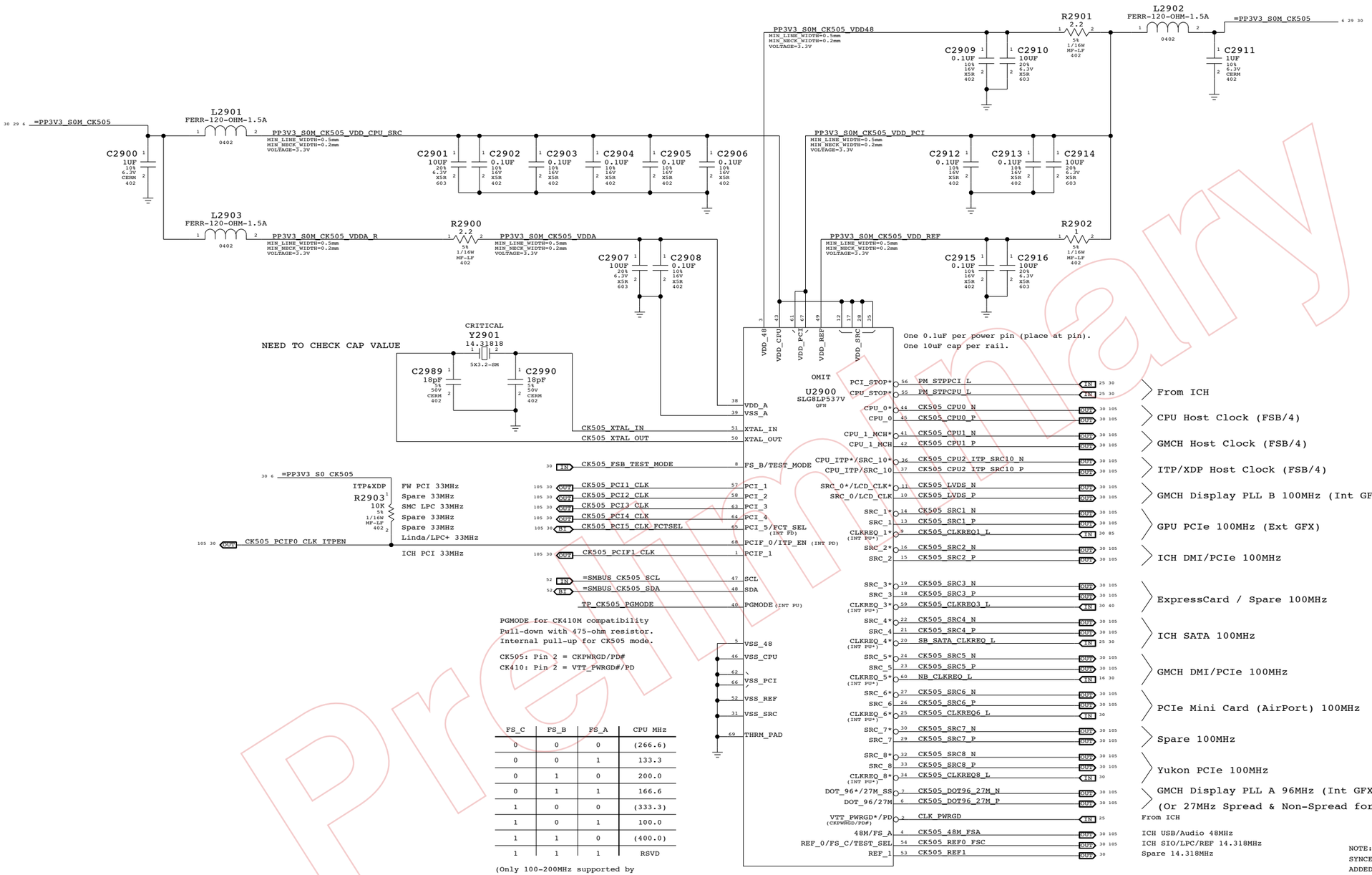
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 28 OF 118	

Preliminary


=PP3V3_S0M_CK505
L2901
FERR-120-OHM-1.5A
PP3V3_S0M_CK505_VDD_CPU_SRC
C2900 1UF
C2901 10UF
C2902 C2903 C2904 C2905 C2906 0.1UF
L2903
FERR-120-OHM-1.5A
PP3V3_S0M_CK505_VDDA_R
R2900 2.2
PP3V3_S0M_CK505_VDDA
C2907 10UF
C2908 0.1UF
PP3V3_S0M_CK505_VDD48
L2902
FERR-120-OHM-1.5A
=PP3V3_S0M_CK505
C2909 0.1UF
C2910 10UF
R2901 2.2
C2911 1UF
PP3V3_S0M_CK505_VDD_PCI
C2912 0.1UF
C2913 0.1UF
C2914 10UF
PP3V3_S0M_CK505_VDD_REF
R2902 1
C2915 0.1UF
C2916 10UF
VDD_48
VDD_CPU
VDD_PCI
VDD_REF
VDD_SRC
One 0.1uF per power pin (place at pin).
One 10uF cap per rail.
CRITICAL
Y2901
14.31818
5X3.2-SM
NEED TO CHECK CAP VALUE
C2989 18pF
C2990 18pF
CK505_XTAL_IN
CK505_XTAL_OUT
VDD_A
VSS_A
XTAL_IN
XTAL_OUT
OMIT
U2900
SLG8LP537V
QFN
PCI_STOP*
CPU_STOP*
PM_STPPCI_L
PM_STPCPU_L
From ICH
CPU_0*
CPU_0
CK505_CPU0_N
CK505_CPU0_P
CPU Host Clock (FSB/4)
CPU_1_MCH*
CPU_1_MCH
CK505_CPU1_N
CK505_CPU1_P
GMCH Host Clock (FSB/4)
CPU_ITP*/SRC_10*
CPU_ITP/SRC_10
CK505_CPU2_ITP_SRC10_N
CK505_CPU2_ITP_SRC10_P
ITP/XDP Host Clock (FSB/4)
SRC_0*/LCD_CLK*
SRC_0/LCD_CLK
CK505_LVDS_N
CK505_LVDS_P
GMCH Display PLL B 100MHz (Int GFX)
SRC_1*
SRC_1
CK505_SRC1_N
CK505_SRC1_P
CLKREQ_1*
CK505_CLKREQ1_L
GPU PCIe 100MHz (Ext GFX)
SRC_2*
SRC_2
CK505_SRC2_N
CK505_SRC2_P
ICH DMI/PCIe 100MHz
SRC_3*
SRC_3
CK505_SRC3_N
CK505_SRC3_P
CLKREQ_3*
CK505_CLKREQ3_L
ExpressCard / Spare 100MHz
SRC_4*
SRC_4
CK505_SRC4_N
CK505_SRC4_P
CLKREQ_4*
SB_SATA_CLKREQ_L
ICH SATA 100MHz
SRC_5*
SRC_5
CK505_SRC5_N
CK505_SRC5_P
CLKREQ_5*
NB_CLKREQ_L
GMCH DMI/PCIe 100MHz
SRC_6*
SRC_6
CK505_SRC6_N
CK505_SRC6_P
CLKREQ_6*
CK505_CLKREQ6_L
PCIe Mini Card (AirPort) 100MHz
SRC_7*
SRC_7
CK505_SRC7_N
CK505_SRC7_P
Spare 100MHz
SRC_8*
SRC_8
CK505_SRC8_N
CK505_SRC8_P
CLKREQ_8*
CK505_CLKREQ8_L
Yukon PCIe 100MHz
DOT_96*/27M_SS
DOT_96/27M
CK505_DOT96_27M_N
CK505_DOT96_27M_P
GMCH Display PLL A 96MHz (Int GFX)
(Or 27MHz Spread & Non-Spread for Ext GFX)
VTT_PWRGD*/PD
CLK_PWRGD
From ICH
48M/FS_A
CK505_48M_FSA
ICH USB/Audio 48MHz
REF_0/FS_C/TEST_SEL
CK505_REF0_FSC
ICH SIO/LPC/REF 14.318MHz
REF_1
CK505_REF1
Spare 14.318MHz
(*) CLKREQ# internal pull-ups only on SLG8LP536/7, not CY28545-5.
=PP3V3_S0_CK505
ITP&XDP
R2903 10K
FW PCI 33MHz
Spare 33MHz
SMC LPC 33MHz
Spare 33MHz
Spare 33MHz
Linda/LPC+ 33MHz
ICH PCI 33MHz
CK505_PCIF0_CLK_ITPEN
CK505_FSB_TEST_MODE
FS_B/TEST_MODE
CK505_PCI1_CLK
CK505_PCI2_CLK
CK505_PCI3_CLK
CK505_PCI4_CLK
CK505_PCI5_CLK_FCTSEL
PCI_1
PCI_2
PCI_3
PCI_4
PCI_5/FCT_SEL
PCIF_0/ITP_EN
CK505_PCIF1_CLK
PCIF_1
=SMBUS_CK505_SCL
=SMBUS_CK505_SDA
SCL
SDA
TP_CK505_PGMODE
PGMODE
PGMODE for CK410M compatibility
Pull-down with 475-ohm resistor.
Internal pull-up for CK505 mode.
CK505: Pin 2 = CKPWRGD/PD#
CK410: Pin 2 = VTT_PWRGD#/PD
VSS_48
VSS_CPU
VSS_PCI
VSS_REF
VSS_SRC
THRM_PAD
FS_C FS_B FS_A CPU MHz
0 0 0 (266.6)
0 0 1 133.3
0 1 0 200.0
0 1 1 166.6
1 0 0 (333.3)
1 0 1 100.0
1 1 0 (400.0)
1 1 1 RSVD
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)
FCT_SEL PIN 6 PIN 7 PIN 10 PIN 11
0 DOT_96+ DOT_96- LCD_CLK+ LCD_CLK- (For Internal Graphics)
1 27M 27M w/SS SRC_0+ SRC_0- (For External Graphics)
NOTE:
SYNCED FROM T9_MLB_NOME
ADDED 475-OHM RESISTOR TO NB_CLKREQ_L PER INTEL
DELETED RES AFTER INTEL SAID IT'S NOT NEEDED!
Clock (CK505)
SYNC_MASTER=JAMES
SYNC_DATE=11/27/2006
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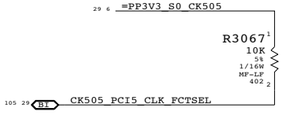
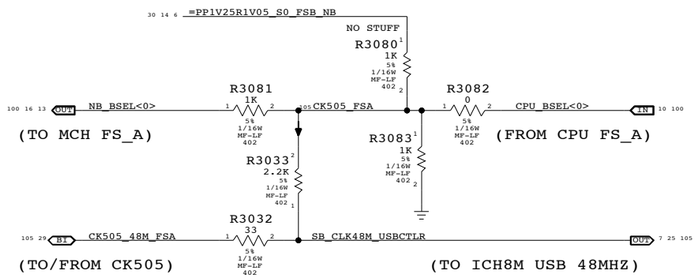
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7228
REV. 27
SCALE NONE
SHT 29 OF 118

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)

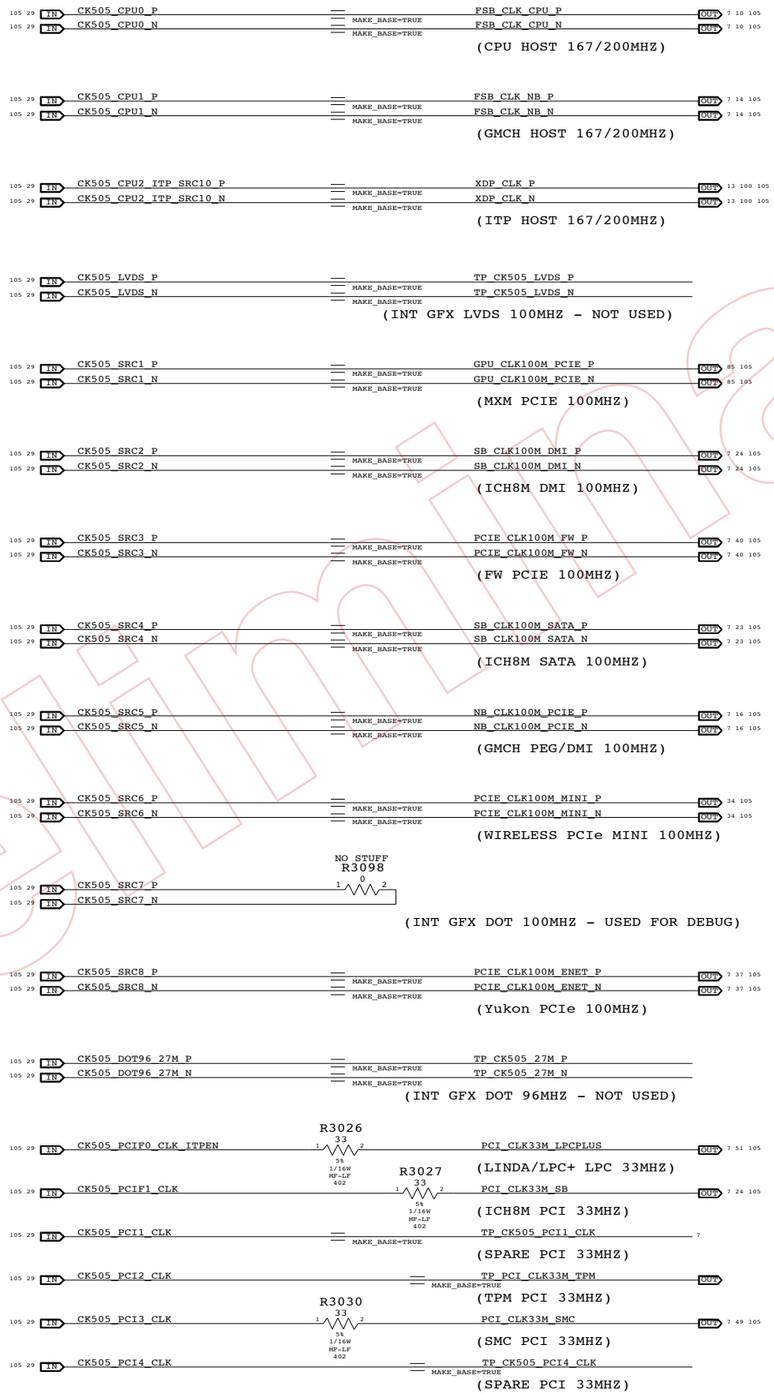


FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

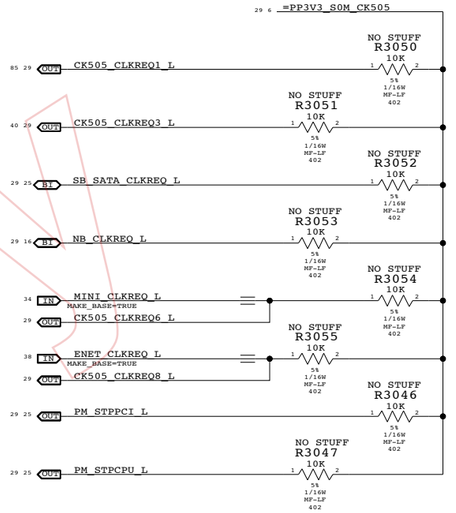
CLK Termination

(Note: HOST/SRC/GFX clock termination kept on T9 for Cypress CY28545-5 compatibility)



CLKREQ Controls

Silego SL8GLP537 has internal
PULL-UPS ON ALL CLKREQ# PINS?



Unused Clocks

(Spare 14.318MHZ)

Clock Termination

SYNC_MASTER=JAMES SYNC_DATE=10/18/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 30 OF 118	

Preliminary

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

=PP0V9_S3_MEM_A_VREF
C3130 2.2UF 20% 6.3V CERM1 603
C3131 0.1uF 20% 10V CERM 402
=PP1V8_S3_MEM

CRITICAL
J3100
F-RT-SM
DDR2-SODIMM-M72

1	VREF		2	VSS0			
3	VSS1		4	DQ4	MEM_A_DQ<4>	17	102
5	DQ0	MEM_A_DQ<0>	6	DQ5	MEM_A_DQ<5>	17	102
7	DQ1	MEM_A_DQ<1>	8	VSS2			
9	VSS4		10	DM0	MEM_A_DM<0>	17	102
11	DQS0*	MEM_A_DQS_N<0>	12	VSS5			
13	DQS0	MEM_A_DQS_P<0>	14	DQ6	MEM_A_DQ<6>	17	102
15	VSS6		16	DQ7	MEM_A_DQ<7>	7 17	102
17	DQ2	MEM_A_DQ<2>	18	VSS7			
19	DQ3	MEM_A_DQ<3>	20	DQ12	MEM_A_DQ<12>	17	102
21	VSS8		22	DQ13	MEM_A_DQ<13>	17	102
23	DQ8	MEM_A_DQ<8>	24	VSS9			
25	DQ9	MEM_A_DQ<9>	26	DM1	MEM_A_DM<1>	17	102
27	VSS10		28	VSS11			
29	DQS1*	MEM_A_DQS_N<1>	30	CK0	MEM_CLK_P<0>	16	102
31	DQS1	MEM_A_DQS_P<1>	32	CK0*	MEM_CLK_N<0>	16	102
33	VSS12		34	VSS13			
35	DQ10	MEM_A_DQ<10>	36	DQ14	MEM_A_DQ<14>	7 17	102
37	DQ11	MEM_A_DQ<11>	38	DQ15	MEM_A_DQ<15>	17	102
39	VSS14		40	VSS15			
KEY							
41	VSS16		42	VSS17			
43	DQ16	MEM_A_DQ<16>	44	DQ20	MEM_A_DQ<20>	17	102
45	DQ17	MEM_A_DQ<17>	46	DQ21	MEM_A_DQ<21>	17	102
47	VSS18		48	VSS19			
49	DQS2*	MEM_A_DQS_N<2>	50	NC0	PM_EXTTS_L<0>	16	49
51	DQS2	MEM_A_DQS_P<2>	52	DM2	MEM_A_DM<2>	17	102
53	VSS21		54	VSS22			
55	DQ18	MEM_A_DQ<18>	56	DQ22	MEM_A_DQ<22>	17	102
57	DQ19	MEM_A_DQ<19>	58	DQ23	MEM_A_DQ<23>	17	102
59	VSS23		60	VSS24			
61	DQ24	MEM_A_DQ<24>	62	DQ28	MEM_A_DQ<28>	17	102
63	DQ25	MEM_A_DQ<25>	64	DQ29	MEM_A_DQ<29>	17	102
65	VSS25		66	VSS26			
67	DM3	MEM_A_DM<3>	68	DQS3*	MEM_A_DQS_N<3>	7 17	102
69	NC1	NC	70	DQS3	MEM_A_DQS_P<3>	7 17	102
71	VSS27		72	VSS28			
73	DQ26	MEM_A_DQ<26>	74	DQ30	MEM_A_DQ<30>	17	102
75	DQ27	MEM_A_DQ<27>	76	DQ31	MEM_A_DQ<31>	17	102
77	VSS29		78	VSS30			
79	CKE0	MEM_CKE<0>	80	NC/CKE1	MEM_CKE<1>	16	33 102
81	VDD0		82	VDD1			
83	NC2	NC	84	NC/A15	TP_MEM_A_A<15>		
85	BA2	MEM_A_BS<2>	86	NC/A14	MEM_A_A<14>	16	33 102
87	VDD2		88	VDD3			
89	A12	MEM_A_A<12>	90	A11	MEM_A_A<11>	17	33 102
91	A9	MEM_A_A<9>	92	A7	MEM_A_A<7>	17	33 102
93	A8	MEM_A_A<8>	94	A6	MEM_A_A<6>	17	33 102
95	VDD4		96	VDD5			
97	A5	MEM_A_A<5>	98	A4	MEM_A_A<4>	17	33 102
99	A3	MEM_A_A<3>	100	A2	MEM_A_A<2>	17	33 102
101	A1	MEM_A_A<1>	102	A0	MEM_A_A<0>	17	33 102
103	VDD6		104	VDD7			
105	A10/AP	MEM_A_A<10>	106	BA1	MEM_A_BS<1>	17	33 102
107	BA0	MEM_A_BS<0>	108	RAS*	MEM_A_RAS_L	17	33 102
109	WE*	MEM_A_WE_L	110	S0*	MEM_CS_L<0>	16	33 102
111	VDD8		112	VDD9			
113	CAS*	MEM_A_CAS_L	114	ODT0	MEM_ODT<0>	16	33 102
115	NC/S1*	MEM_CS_L<1>	116	NC/A13	MEM_A_A<13>	17	33 102
117	VDD10		118	VDD11			
119	NC/ODT1	MEM_ODT<1>	120	NC3	NC		
121	VSS31		122	VSS32			
123	DQ32	MEM_A_DQ<32>	124	DQ36	MEM_A_DQ<36>	17	102
125	DQ33	MEM_A_DQ<33>	126	DQ37	MEM_A_DQ<37>	17	102
127	VSS33		128	VSS34			
129	DQS4*	MEM_A_DQS_N<4>	130	DM4	MEM_A_DM<4>	17	102
131	DQS4	MEM_A_DQS_P<4>	132	VSS35			
133	VSS36		134	DQ38	MEM_A_DQ<38>	17	102
135	DQ34	MEM_A_DQ<34>	136	DQ39	MEM_A_DQ<39>	7 17	102
137	DQ35	MEM_A_DQ<35>	138	VSS37			
139	VSS38		140	DQ44	MEM_A_DQ<44>	17	102
141	DQ40	MEM_A_DQ<40>	142	DQ45	MEM_A_DQ<45>	17	102
143	DQ41	MEM_A_DQ<41>	144	VSS39			
145	VSS40		146	DQS5*	MEM_A_DQS_N<5>	7 17	102
147	DM5	MEM_A_DM<5>	148	DQS5	MEM_A_DQS_P<5>	7 17	102
149	VSS41		150	VSS42			
151	DQ42	MEM_A_DQ<42>	152	DQ46	MEM_A_DQ<46>	17	102
153	DQ43	MEM_A_DQ<43>	154	DQ47	MEM_A_DQ<47>	7 17	102
155	VSS43		156	VSS44			
157	DQ48	MEM_A_DQ<48>	158	DQ52	MEM_A_DQ<52>	17	102
159	DQ49	MEM_A_DQ<49>	160	DQ53	MEM_A_DQ<53>	17	102
161	VSS45		162	VSS46			
163	NC_TEST	NC	164	CK1	MEM_CLK_P<1>	16	102
165	VSS47		166	CK1*	MEM_CLK_N<1>	16	102
167	DQS6*	MEM_A_DQS_N<6>	168	VSS48			
169	DQS6	MEM_A_DQS_P<6>	170	DM6	MEM_A_DM<6>	17	102
171	VSS49		172	VSS50			
173	DQ50	MEM_A_DQ<50>	174	DQ54	MEM_A_DQ<54>	7 17	102
175	DQ51	MEM_A_DQ<51>	176	DQ55	MEM_A_DQ<55>	17	102
177	VSS51		178	VSS52			
179	DQ56	MEM_A_DQ<56>	180	DQ60	MEM_A_DQ<60>	17	102
181	DQ57	MEM_A_DQ<57>	182	DQ61	MEM_A_DQ<61>	17	102
183	VSS53		184	VSS54			
185	DM7	MEM_A_DM<7>	186	DQS7*	MEM_A_DQS_N<7>	7 17	102
187	VSS55		188	DQS7	MEM_A_DQS_P<7>	7 17	102
189	DQ58	MEM_A_DQ<58>	190	VSS56			
191	DQ59	MEM_A_DQ<59>	192	DQ62	MEM_A_DQ<62>	17	102
193	VSS57		194	DQ63	MEM_A_DQ<63>	17	102
195	SDA	=I2C_DIMMA_SDA	196	VSS58	ADDR=0xA0(WR)/0xA1(RD)		
197	SCL	=I2C_DIMMA_SCL	198	SA0	MEM_A_SA<0>		
199	VDDSPD		200	SA1	MEM_A_SA<1>		
201	GND						
202	GND						
203	GND						
204	GND						
205	GND						

516S0565

R3140 10K 1/16W 5% MF-LF 402
R3141 10K 1/16W 5% MF-LF 402

=PP1V8_S3_MEM
R3100 1K 1% 1/16W MF-LF 402
PP0V9_S3_MEM_A_VREF (VOLTAGE=0.9V TRUE MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.25MM) =PP0V9_S3_MEM_A_VREF
R3101 1K 1% 1/16W MF-LF 402

DDR2 Bypass Caps
(For return current)

=PP1V8_S3_MEM
C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 1UF 10% 6.3V CERM 402
C3111 1UF 10% 6.3V CERM 402
C3112 1UF 10% 6.3V CERM 402
C3113 1UF 10% 6.3V CERM 402
C3114 1UF 10% 6.3V CERM 402
C3115 1UF 10% 6.3V CERM 402
C3116 1UF 10% 6.3V CERM 402
C3117 1UF 10% 6.3V CERM 402
C3118 1UF 10% 6.3V CERM 402
C3119 1UF 10% 6.3V CERM 402
C3120 1UF 10% 6.3V CERM 402
C3121 1UF 10% 6.3V CERM 402
C3122 1UF 10% 6.3V CERM 402
C3123 1UF 10% 6.3V CERM 402

=PPSPD_S0_MEM
C3140 2.2UF 20% 6.3V CERM1 603
C3141 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=JAMES SYNC_DATE=10/17/06

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT: 31 OF: 118	

Preliminary

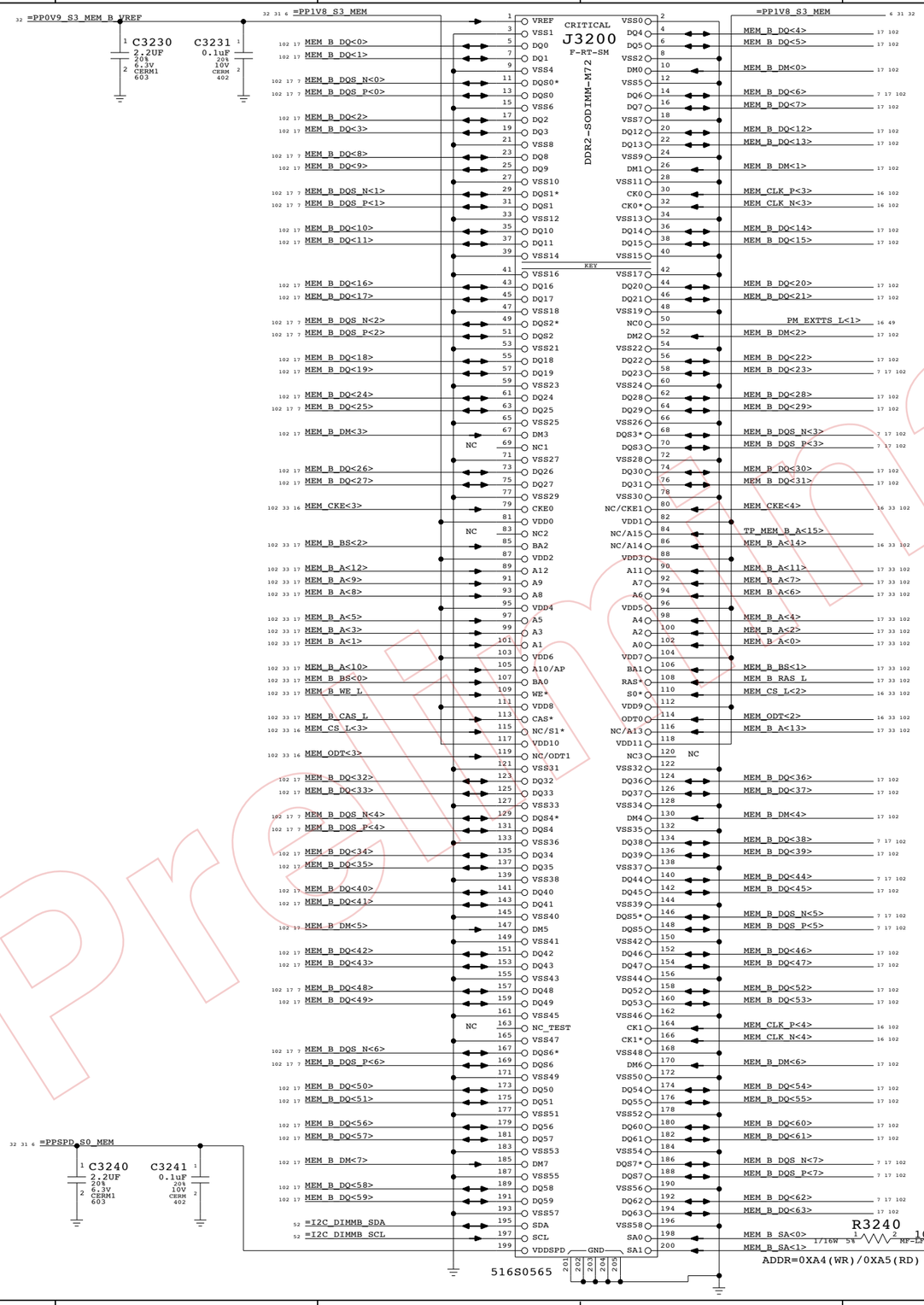
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

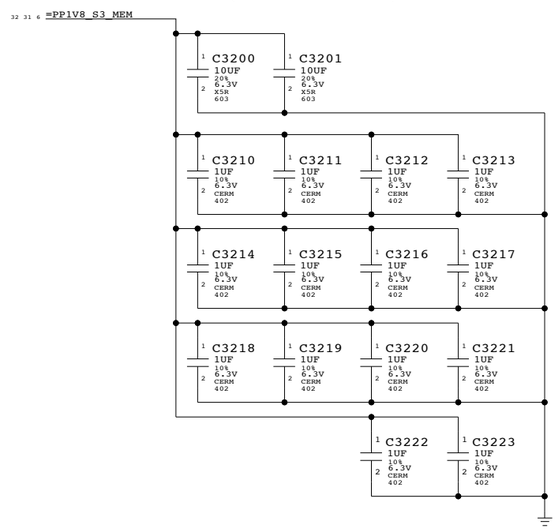
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=JAMES SYNC_DATE=10/17/06

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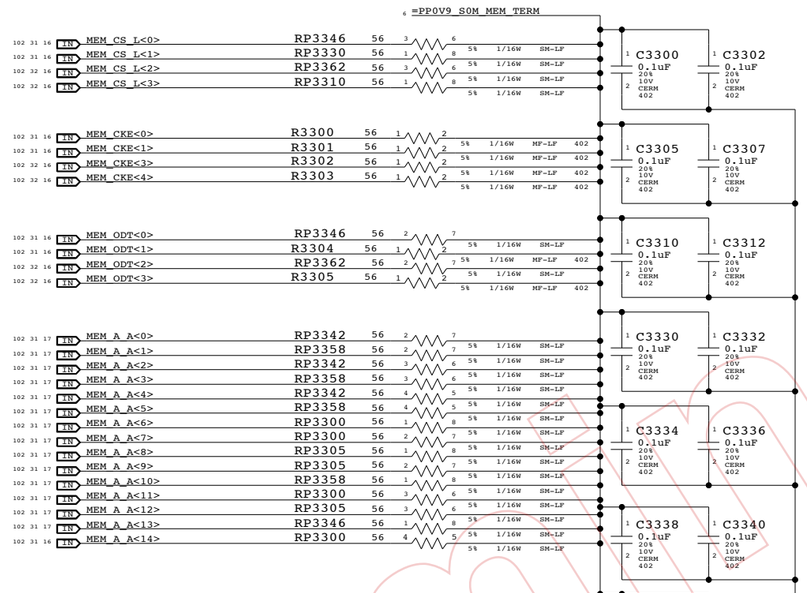
SCALE: NONE	SHT: 32 OF 118	

Preliminary

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=JAMES SYNC_DATE=12/04/2006

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SCALE	SHT	OF
NONE	33	118

Preliminary

3.3V_S3_CURRENT	D0-D2,D3HOT	D3COLD
MAX CONT.	1100MA	250MA
MAX PEAK	2750MA	2750MA
1.5V_CURRENT		
MAX CONT.	375MA	N/A
MAX PEAK	500MA	N/A

NOTE: CURRENT DATA PER 5/16/2005 PCIE MINI CEM ECN

NO STUFF
R3400
0
5% 1/16W MF-LF 402

NO STUFF
R3401
0
5% 1/16W MF-LF 402

CRITICAL
J3400
ASOB226-S80N-7F
F-RT-SM

37 25 OUT PCIE_WAKE_L
RSVD_MINI_WLAN_ACTIVE
RSVD_MINI_BT_ACTIVE
30 OUT MINI_CLKREQ_L
105 30 IN PCIE_CLK100M_MINI_N
105 30 IN PCIE_CLK100M_MINI_P
RESERVED
RESERVED
MINI_RESET_L IN 28
=SMBUS_MINI_SCL IN 32
=SMBUS_MINI_SDA BI 32
USB_MINI_N BI 24 103
USB_MINI_P BI 24 103
PP1V05_S0 6 7 73
=PP3V3_S3_MINI 6
=PP1V5_S0_MINI 6

NC pins: 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52

516S0391

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603
C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

104 24 7 OUT PCIE_MINI_D2R_N
104 24 7 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=Place close to U2300.
C3431
0.1uF
104 24 IN PCIE_MINI_R2D_C_N
10% 16V X5R 402

PLACEMENT_NOTE=Place close to U2300.
C3430
0.1uF
104 24 IN PCIE_MINI_R2D_C_P
10% 16V X5R 402

109 PCIE_MINI_R2D_N
109 PCIE_MINI_R2D_P

CLINK_WLAN_CLK = TP_CLINK_WLAN_CLK MAKE_BASE=TRUE
CLINK_WLAN_DATA = TP_CLINK_WLAN_DATA MAKE_BASE=TRUE
CLINK_WLAN_RESET_L = TP_CLINK_WLAN_RESET_L MAKE_BASE=TRUE

25
25 28
25

STANDOFF FOR J3400

SDF3400
STDOFF-4OD5.6H-1.35-TH
SDF3400_1
860-0691

R3410
0
5% 1/16W MF-LF 402

PCI-E MiniCard Connector

SYNC_MASTER=DOUG SYNC_DATE=10/30/2006

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Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V9R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

38 =PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

38 =PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

38 =PP1V9R2V5_ENET_PHY — R3720 0 5% 1/16W MF-LF 402 — 104 39 PP1V9R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
(EC:2.5V)

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

38 =YUKON_EC_PP2V5_ENET

104 24 7 OUTPUT PCIE_ENET_D2R_P — C3735 0.1UF 10% 16V X5R 402 — 109 PCIE_ENET_D2R_C_P
104 24 7 OUTPUT PCIE_ENET_D2R_N — C3736 0.1UF 10% 16V X5R 402 — 109 PCIE_ENET_D2R_C_N
PLACEMENT_NOTE=Place C3730 close to southbridge.
104 24 INPUT PCIE_ENET_R2D_C_P — C3730 0.1uF 10% 16V X5R 402 — 109 7 PCIE_ENET_R2D_P
104 24 INPUT PCIE_ENET_R2D_C_N — C3731 0.1uF 10% 16V X5R 402 — 109 7 PCIE_ENET_R2D_N
PLACEMENT_NOTE=Place C3731 close to southbridge.
105 30 7 INPUT PCIE_CLK100M_ENET_P
105 30 7 INPUT PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
38 OUTPUT =ENET_CLKREQ_L
34 25 OUTPUT PCIE_WAKE_L
28 7 INPUT ENET_RESET_L

104 39 BI ENET_MDI_P<0> — R3740 49.9 1% 1/16W MF-LF 402 — ENET_MDI0 — C3740 0.001UF 10% 50V CERM 402
104 39 BI ENET_MDI_N<0>
104 39 BI ENET_MDI_P<1> — R3741 49.9 1% 1/16W MF-LF 402 — ENET_MDI1 — C3742 0.001UF 10% 50V CERM 402
104 39 BI ENET_MDI_N<1>
104 39 BI ENET_MDI_P<2> — R3742 49.9 1% 1/16W MF-LF 402 — R3743 49.9 1% 1/16W MF-LF 402 — ENET_MDI2 — C3744 0.001UF 10% 50V CERM 402
104 39 BI ENET_MDI_N<2>
104 39 BI ENET_MDI_P<3> — R3744 49.9 1% 1/16W MF-LF 402 — R3745 49.9 1% 1/16W MF-LF 402 — ENET_MDI3 — C3746 0.001UF 10% 50V CERM 402
104 39 BI ENET_MDI_N<3> — R3746 49.9 1% 1/16W MF-LF 402 — R3747 49.9 1% 1/16W MF-LF 402

ENET_CLK25M_XTALI — C3750 27PF 5% 50V CERM 402 — CRITICAL Y3750 25.0000M SM-3-LF — ENET_CLK25M_XTALO — C3751 27PF 5% 50V CERM 402

U3700 88E8058 QFN — CRITICAL — OMIT

NC_32	32		
NC_51	51		
NC_52	52		
NC_57	57		
NC_64	64		
AVDD0	19	EC:AVDD 2.5V	
AVDD1	22		
AVDD2	23		
AVDD3	20		
VDDO_TTL0	1		
VDDO_TTL1	40		
VDDO_TTL2	45		
VDDO_TTL3	61		
AVDDH	8		
VDD0	2		
VDD1	7		
VDD2	13		
VDD3	33		
VDD4	39		
VDD5	44		
VDD6	48		
VDD7	58		
TX_P	49		
TX_N	50		
RX_P	54		
RX_N	53		
REFCLKP	55		
REFCLKN	56		
CLKREQ*	42	EC:NO CONNECT	
WAKE*	6		
PERST*	7		
MDIP0	17		
MDIN0	18		
MDIP1	20		
MDIN1	21		
MDIP2	26		
MDIN2	27		
MDIP3	30		
MDIN3	31		
XTALI	15		
XTALO	14		
THRML_PAD	65		

PCI EXPRESS

ANALOG — EC:CTRL25

LOM_DISABLE*	10	ENET_LOM_DIS_L	
VAUX_AVLBL	12		
SWITCH_VAUX	9	NC	
VMAIN_AVLBL	47	=ENET_VMAIN_AVLBL	IN 38
SWITCH_VCC	11	NC	
CTRL18	4	TP_YUKON_CTRL18	OUT 38
CTRL12	3	TP_YUKON_CTRL12	OUT 38
RSET	16	YUKON_RSET	

R3760 4.7K 5% 1/16W MF-LF 402

Must be high in S0 state (can use PP3V3_S0 as input)

YUKON_ULTRA — R3765 4.99K 1% 1/16W MF-LF 402

LED

LED_ACT*	59	ENET_LED_ACT_L	39
LED_LINK10/100*	60	ENET_LED_LINK10_100_L	39
LED_LINK1000*	62	ENET_LED_LINK1000_L	39
LED_DUPLEX*	63	ENET_LED_LINK_L	39

SPI

(IPU) SPI_DO	34	NC	
(IPU) SPI_DI	35	NC	
(IPU) SPI_CLK	37	NC	
(IPU) SPI_CS	36	NC	

MEDIA

TWSI

(IPU) VPD_CLK	38	YUKON_VPD_CLK	
(IPU) VPD_DATA	41	YUKON_VPD_DATA	

TEST/RSVD

(IPD) TESTMODE	46		
RSVD_24	24	NC	
RSVD_25	25	NC	
RSVD_29	29	NC	
RSVD_43	43	NC	

MAIN CLK

VPD ROM

C3780 0.1UF 10% 16V X5R 402

R3780 4.7K 5% 1/16W MF-LF 402; R3781 4.7K 5% 1/16W MF-LF 402

U3780 M24C08 SO8 — OMIT — CRITICAL VSS

E2	3		
NC1	2	NC	
NC0	1	NC	
WC*	7		
VCC	8		
SDA	5		
SCL	6		
VSS	4		

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
- ALIAS =YUKON_EC_PP2V5_ENET TO PP1V9R2V5_ENET_PHY_AVDD, ADD 1X 0.1UF AND 1X 0.001UF CAPS
- USE 0-OHM RESISTORS OR VARIABLE SUPPLY TO PROVIDE 1.8V OR 2.5V TO =PP1V9R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=DOUG SYNC_DATE=11/08/2006

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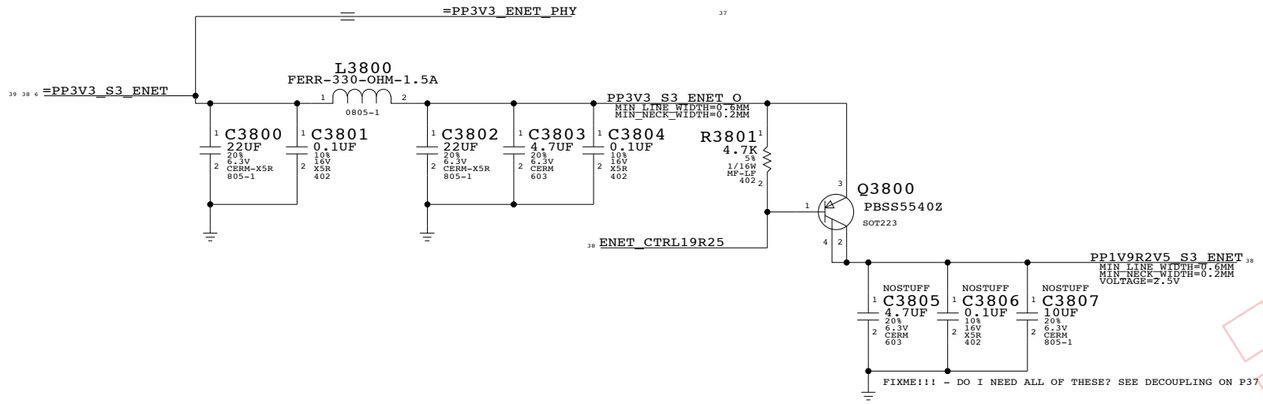
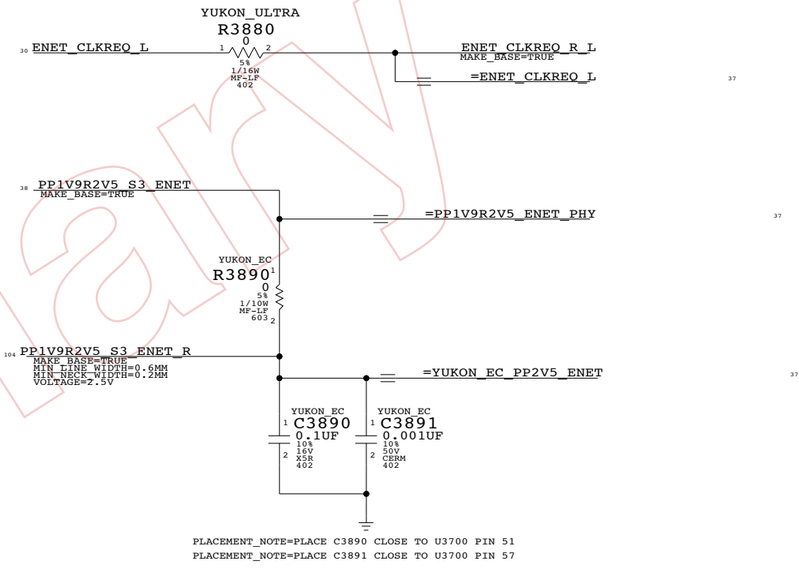
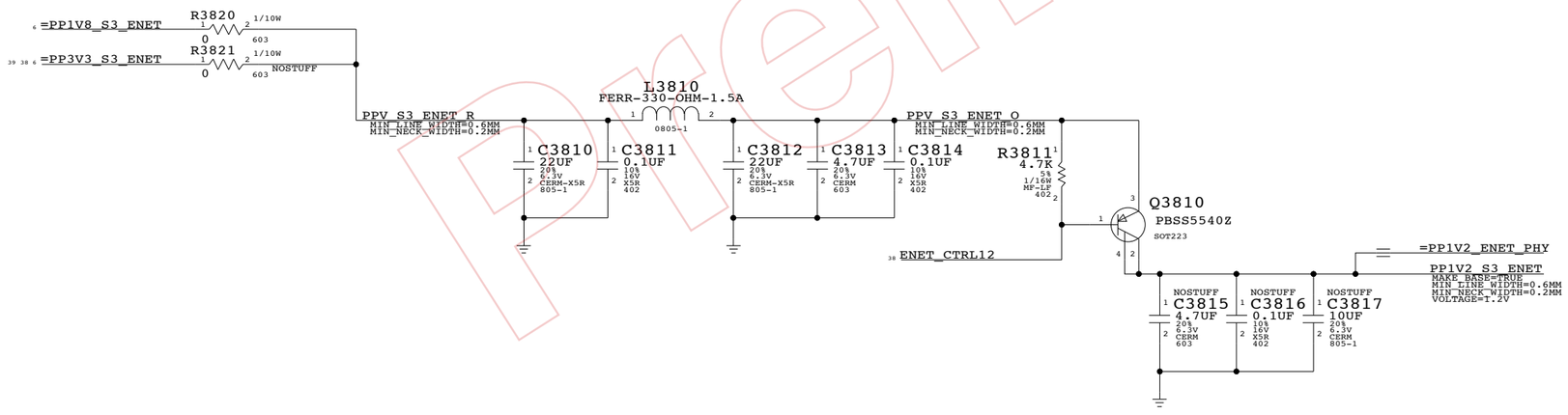
YUKON 1.9/2.5 RAIL SUPPLY



YUKON EC / YUKON ULTRA SUPPORT



YUKON 1.2 RAIL SUPPLY



YUKON T9 ALIASES

TP_YUKON_CTRL18 = ENET_CTRL19R25 (MAKE_BASE=TRUE)

TP_YUKON_CTRL12 = ENET_CTRL12 (MAKE_BASE=TRUE)

=ENET_VMAIN_AVLBL = =PP3V3_S0_ENET

Preliminary

YUKON/ULTRA SUPPORT

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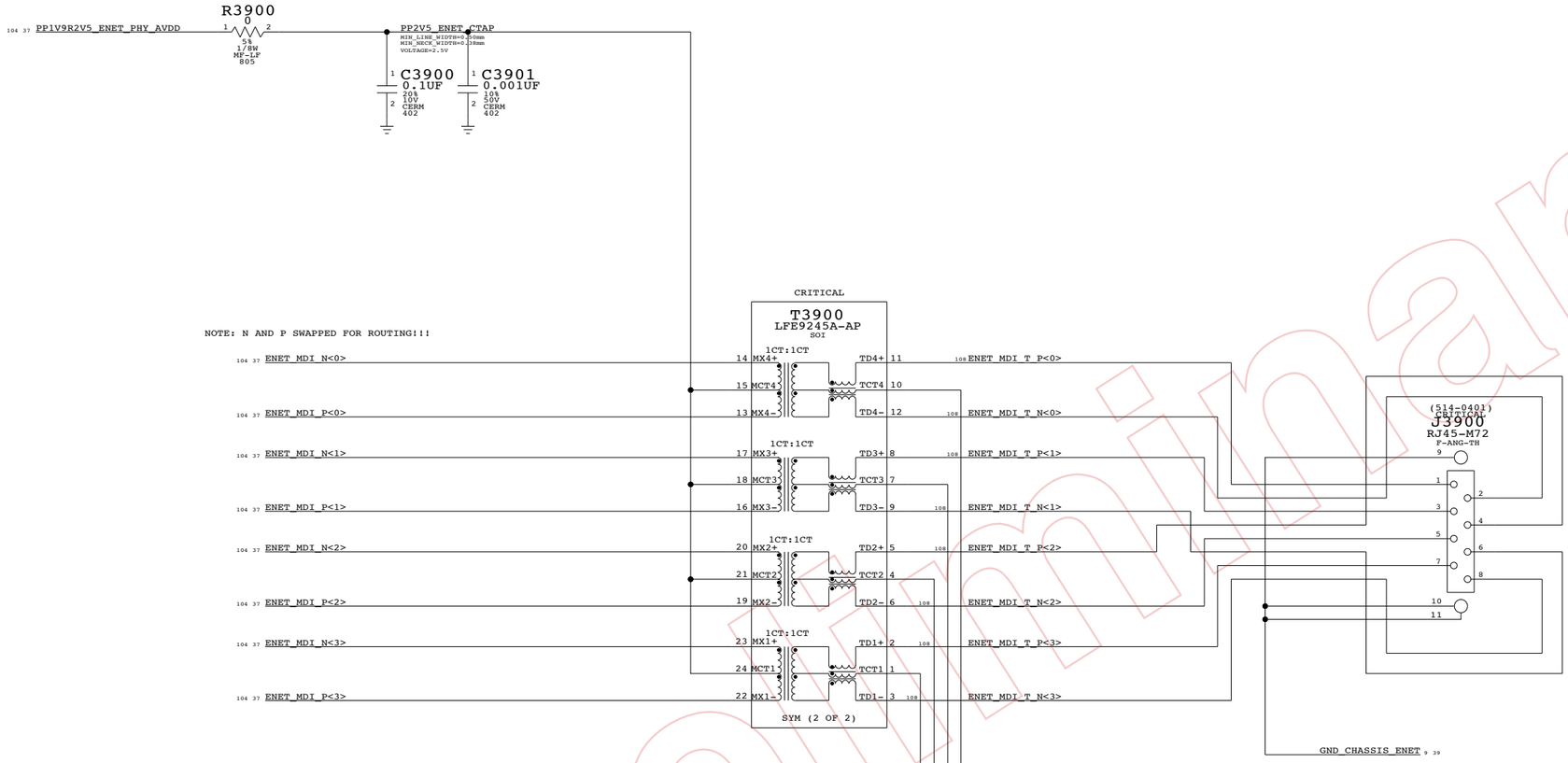
SCALE	SHT	OF
NONE	38	118



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ETHERNET CONNECTOR

SYNC_MASTER=DOUG SYNC_DATE=11/06/2006

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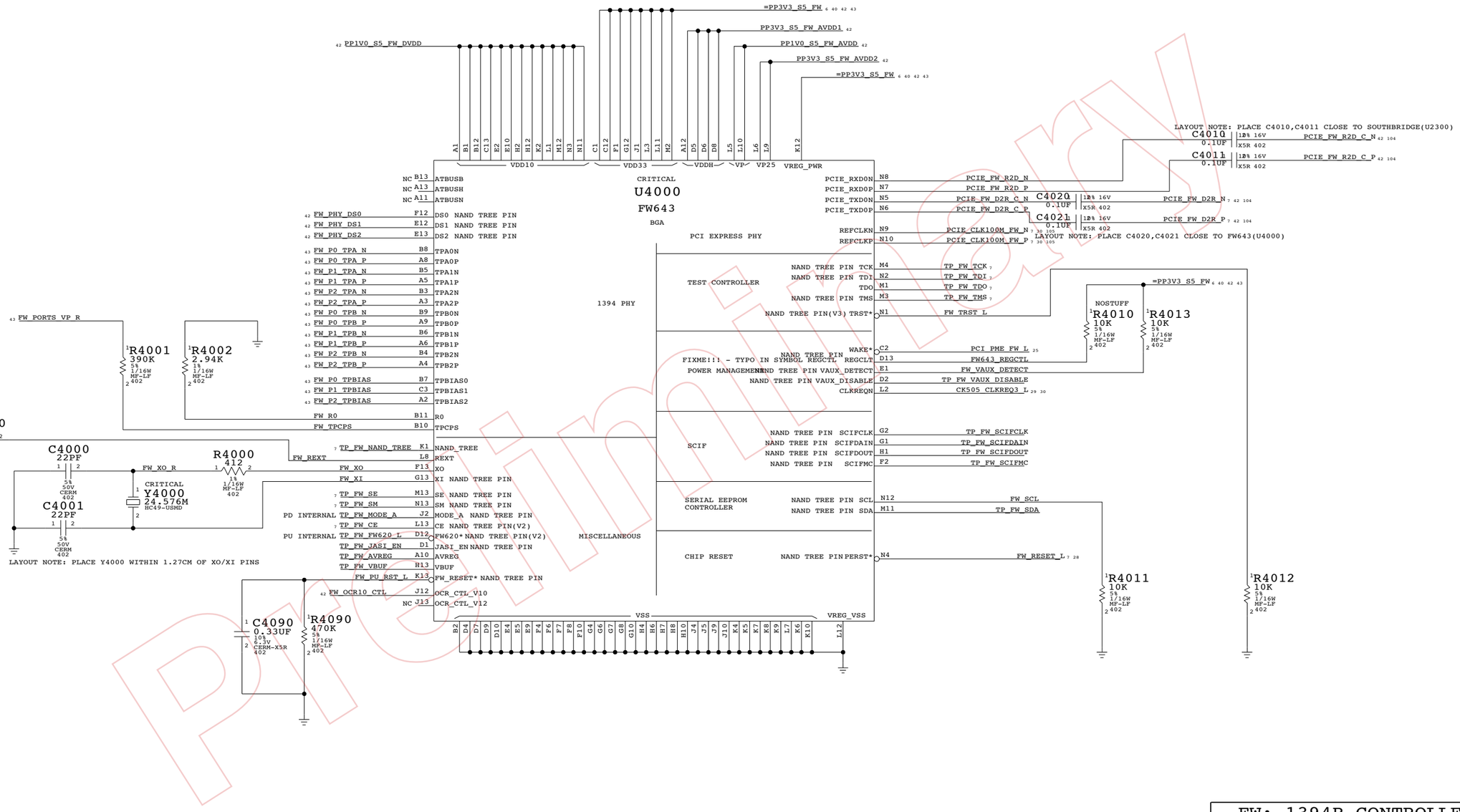

Preliminary

FW: 1394B CONTROLLER

SYNC_MASTER=M78_MLB SYNC_DATE=12/15/2006

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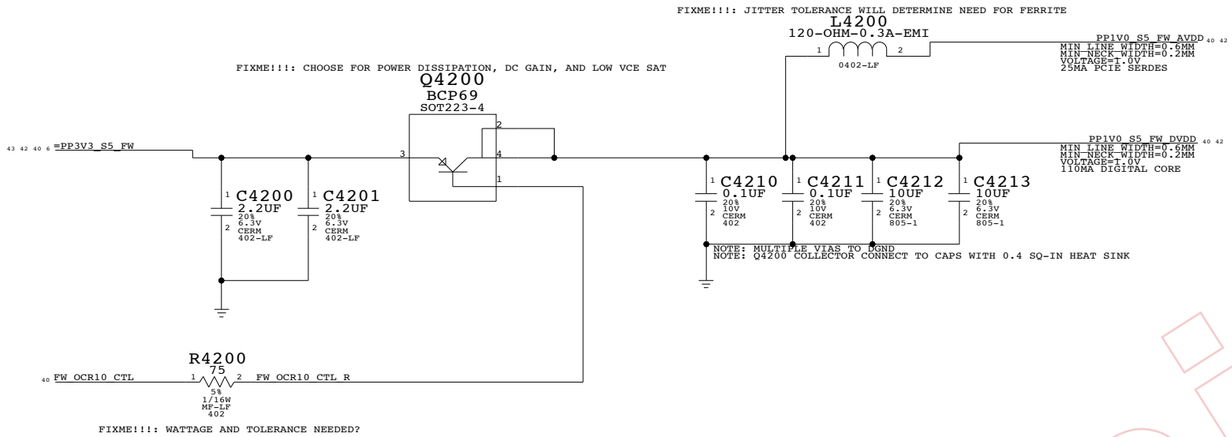
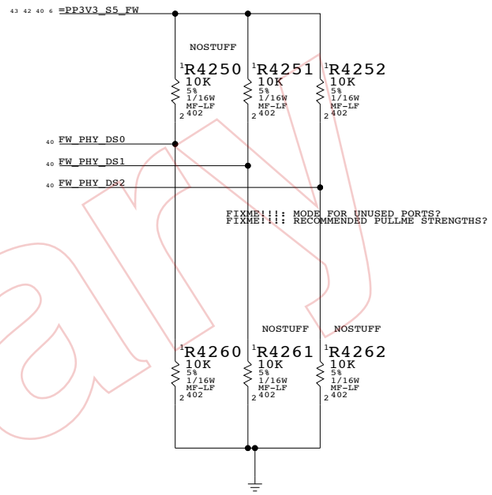
FW643 1.0V GENERATION

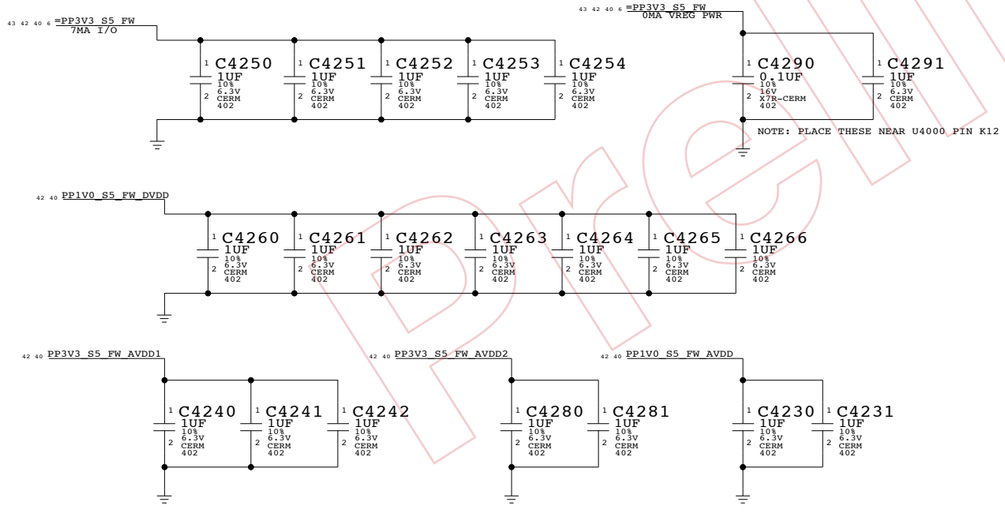


1394 PHY DATA/STROBE OPTIONS

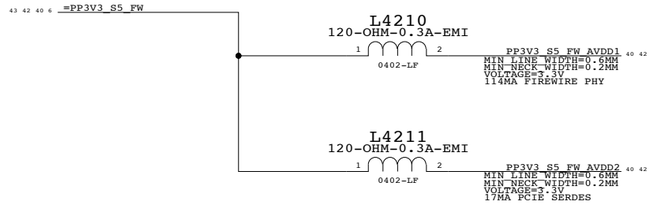


FW643 DECOUPLING

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000



FW 3.3V FILTERING



FW PCIE ALIASES

TP_PCIE_FW_R2D_C_N	MAKE_BASE=TRUE	PCIE_FW_R2D_C_N	
TP_PCIE_FW_R2D_C_P	MAKE_BASE=TRUE	PCIE_FW_R2D_C_P	
PCIE_FW_D2R_N	MAKE_BASE=TRUE	TP_PCIE_FW_D2R_N	
PCIE_FW_D2R_P	MAKE_BASE=TRUE	TP_PCIE_FW_D2R_P	

FW: 1394B MISC

SYNC_MASTER=DOUG SYNC_DATE=10/10/2006

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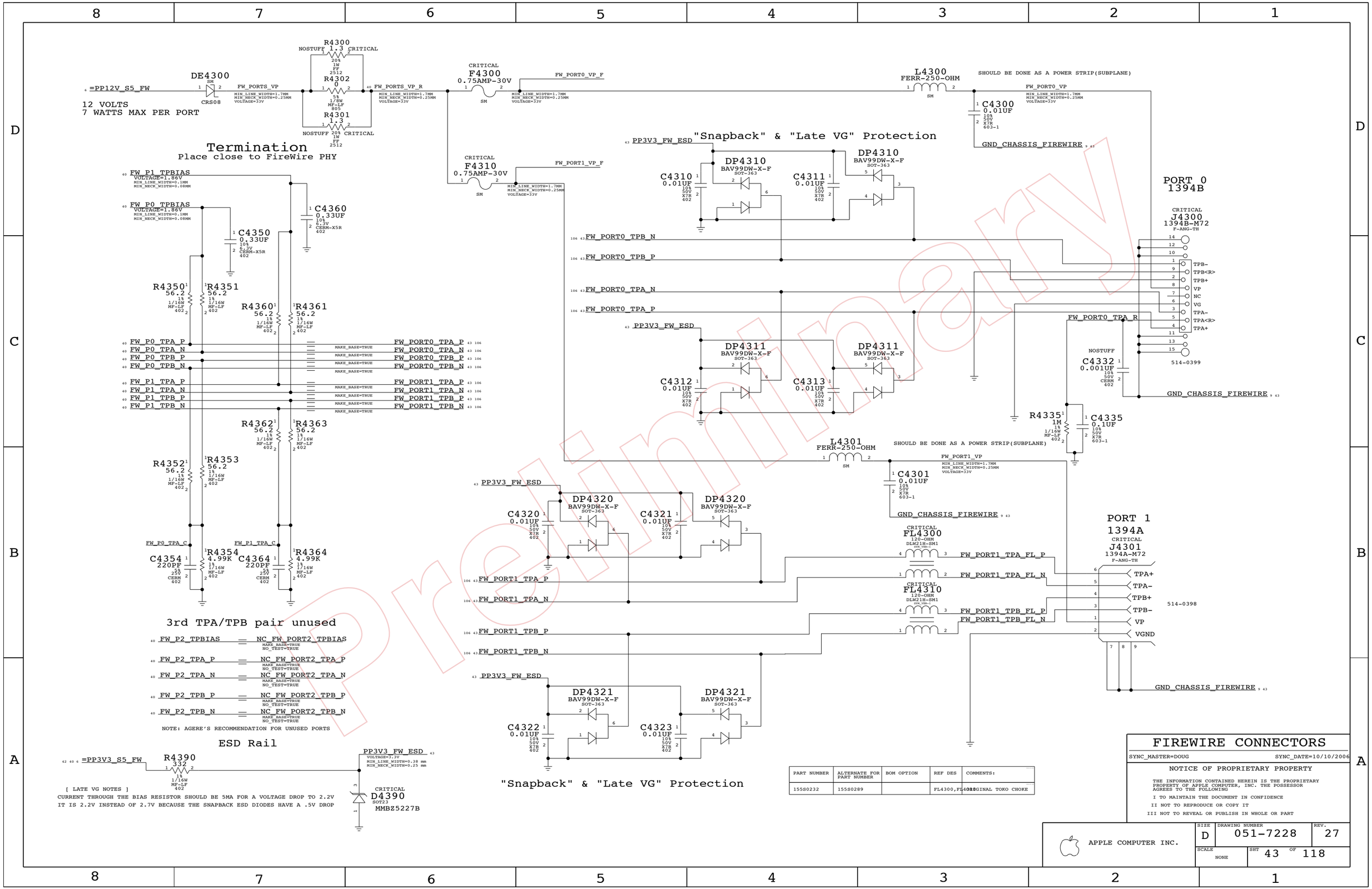

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4300,FL4310	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

SYNC_MASTER=DOUG SYNC_DATE=10/10/2006

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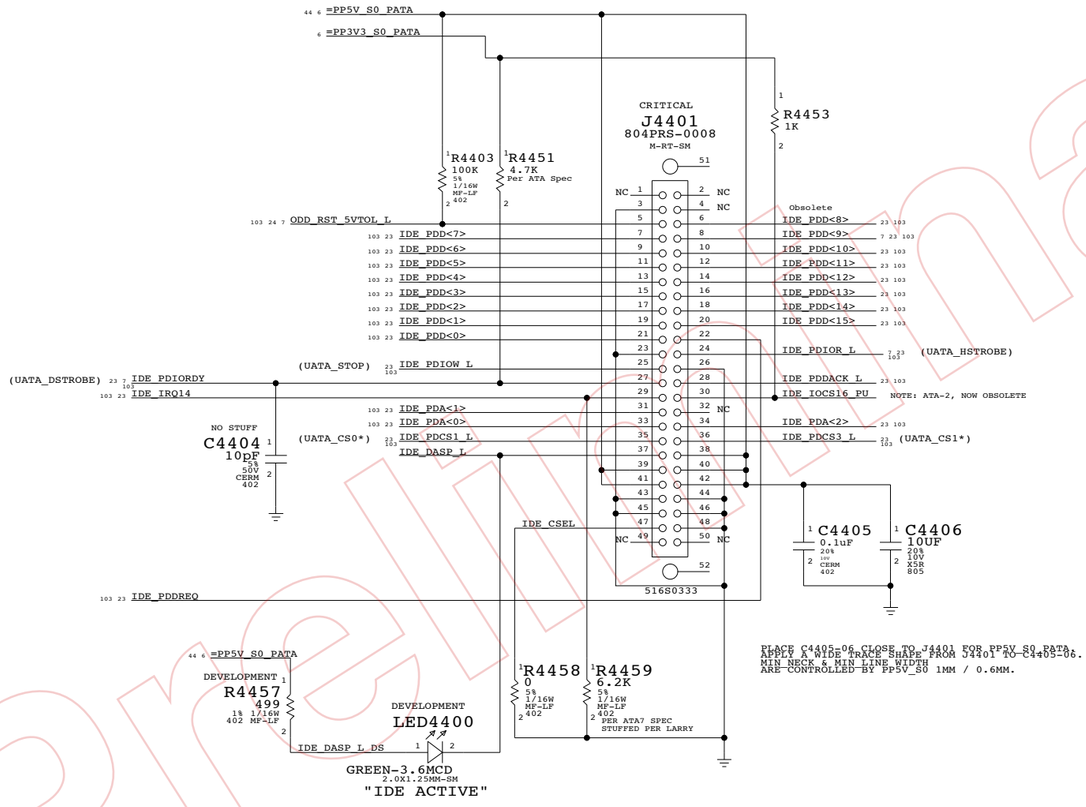
IDE (ODD) Connector



Preliminary

PATA Connector

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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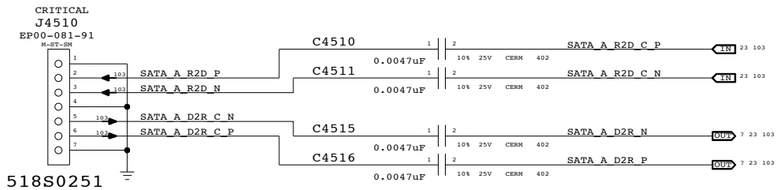
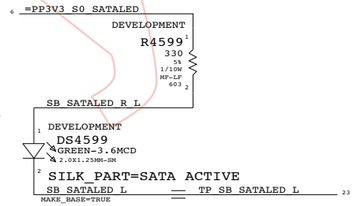
SCALE: NONE	SHT 44 OF 118	

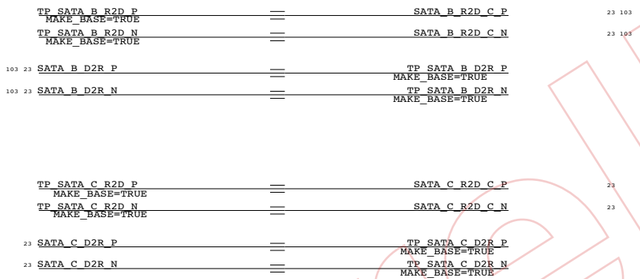
SATA Port A



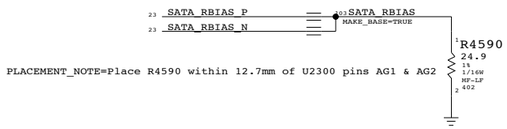
SATA Activity LED



UNUSED SATA PORTS



ICH SATA Support



PLACEMENT_NOTE=Place R4590 within 12.7mm of U2300 pins AG1 & AG2

Preliminary

SATA Connectors

SYNC_MASTER=DOUG SYNC_DATE=10/10/2006

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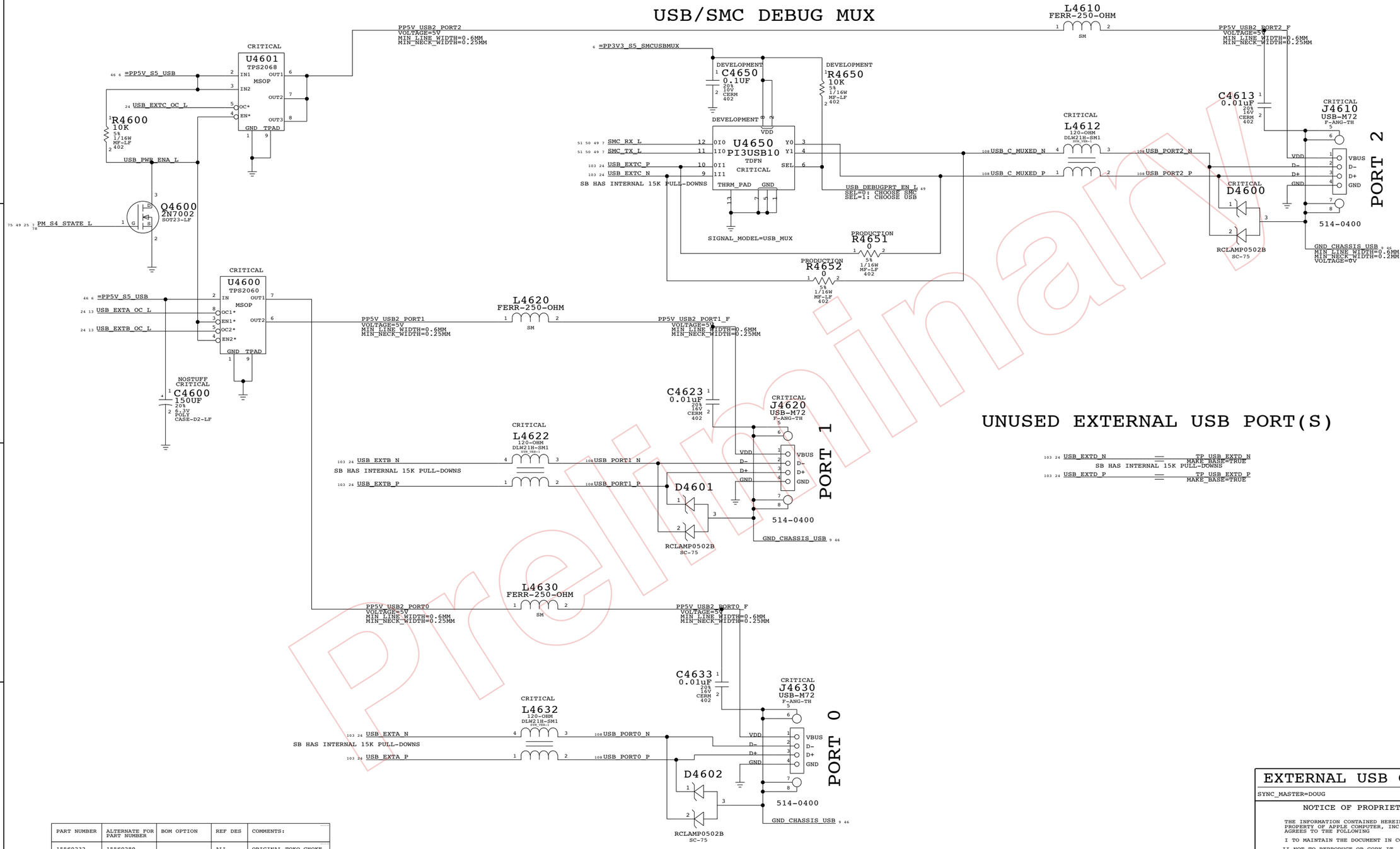
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE NONE SHT 45 OF 118

USB/SMC DEBUG MUX



UNUSED EXTERNAL USB PORT(S)

USB_EXTD_N — TP_USB_EXTD_N — MAKE_BASE=TRUE
SB HAS INTERNAL 15K PULL-DOWNS
USB_EXTD_P — TP_USB_EXTD_P — MAKE_BASE=TRUE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TOKO CHOKE

EXTERNAL USB CONNECTORS

SYNC_MASTER=DOUG SYNC_DATE=12/11/2006

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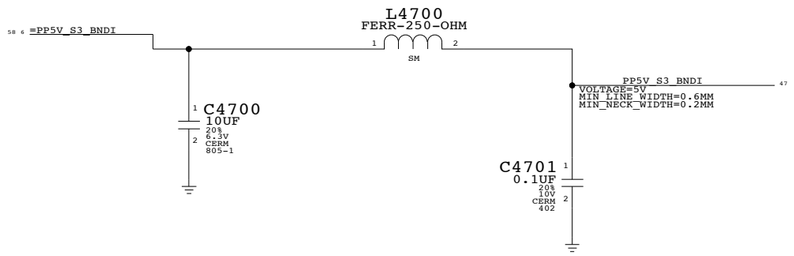
SIZE D | DRAWING NUMBER 051-7228 | REV. 27

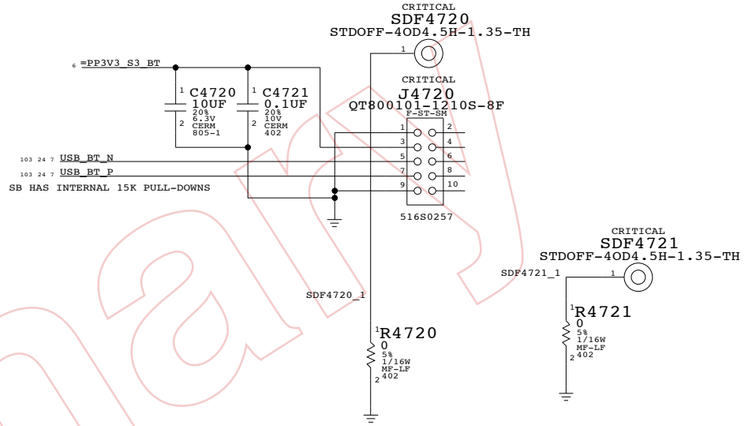
SCALE NONE | SHT 46 OF 118

CAMERA POWER FILTERING

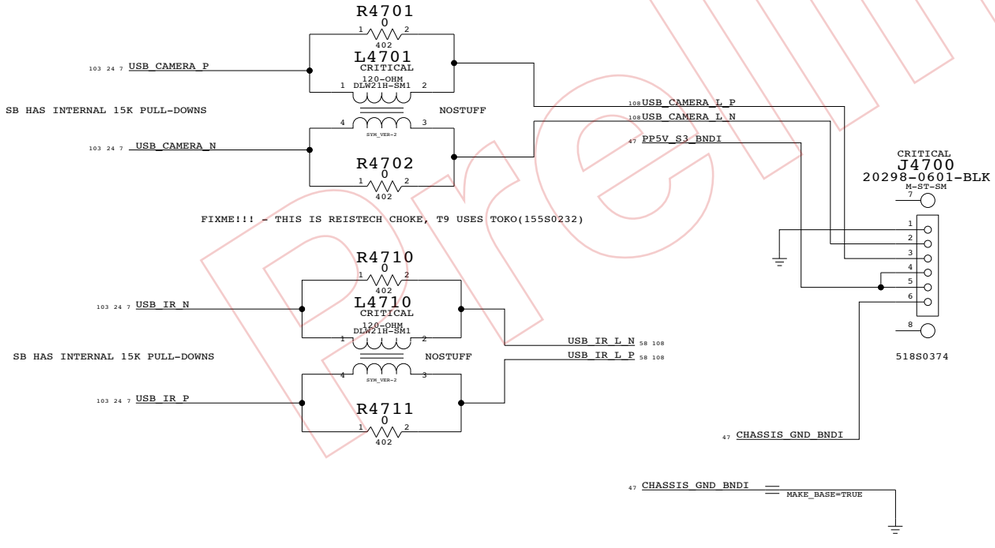


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

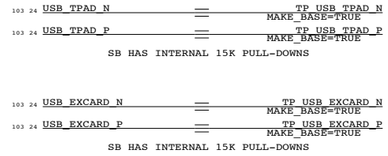
M13D (Bluetooth) Connector



CAMERA CONNECTOR



UNUSED INTERNAL USB PORTS



Preliminary

Internal USB Connections

SYNC_MASTER=M78_MLB SYNC_DATE=12/15/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 47 OF 118	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

OMIT
U4900
SMC_H8S2116
BGA
(1 OF 4)

25	OUT	PM_LAN_ENABLE	B12	P10			
50	OUT	SMC_RSTGATE_L	C13	P11			
84 70 50 7	IN	ALL_SYS_PWRGD	A15	P12			
70	IN	RSMRST_PWRGD	B14	P13			
50		SMC_P14	B15	P14			
25	OUT	PM_RSMRST_L	C14	P15			
71 7	OUT	IMVP_VR_ON	D12	P16			
25	OUT	PM_PWRBTN_L	C15	P17			
		SMC_P20	D13	P20			
50		SMC_P21	D14	P21			
50		SMC_P22	D15	P22			
50		SMC_P23	E12	P23			
50	OUT	SMC_BATT_TRICKLE_EN_L	E14	P24			
50	OUT	SMC_BATT_CHG_EN	E15	P25			
50		SMC_P26	E13	P26			
50		SMC_P27	F14	P27			
51 23 7	BI	LPC_AD<0>	D9	P30/LAD0			
51 23 7	BI	LPC_AD<1>	C9	P31/LAD1			
51 23 7	BI	LPC_AD<2>	A9	P32/LAD2			
51 23 7	BI	LPC_AD<3>	B9	P33/LAD3			
51 23 7	IN	LPC_FRAME_L	D8	P34/LFRAME*			
28 7	IN	SMC_LRESET_L	C8	P35/LRESET*			
105 30 7	IN	PCI_CLK33M_SMC	A8	P36/LCLK			
51 25 7	BI	INT_SERIRQ	D7	P37/SERIRQ			
85	OUT	SMC_GFX_THROTTLE_L	A5	P40/TMIO			
50	OUT	SMC_SYS_LED	B5	P41/TMO0			
52	BI	SMB_MGMT_DATA	(OC) D5	P42/SDA1			
50		SMC_P43	C3	P43/TMI1/EXSCK1			
50		SMC_P44	B1	P44/TMO1			
50		SMC_P45	C2	P45			
50		SMC_P46	D3	P46/PWX0/PWM0			
50	OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1			
51 50 49 46 7	OUT	SMC_TX_L	G1	P50			
51 50 49 46 7	IN	SMC_RX_L	G4	P51			
52	BI	SMB_0_S0_CLK	(OC) F2	P52/SCL0			
		P60/KIN0*	L13	SMC_PM_G2_EN	OUT	50	
		P61/KIN1*	L14	SMC_ADAPTER_EN	OUT	50	
		P62/KIN2*	L15	SMC_P62		50	
		P63/KIN3*	K12	SMC_P63		50	
		P64/KIN4*	K13	SMC_P64		50	
		P65/KIN5*	K14	PM_LAN_PWRGD	IN	50	
		P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L	IN	50	
		P67/IRQ7*/KIN7*	J13	SMC_P67		50	
		P70/AN0	N12	SMC_CPU_ISENSE	IN	53	
		P71/AN1	R13	SMC_CPU_VSENSE	IN	53	
		P72/AN2	P13	SMC_GPU_ISENSE	IN	53	
		P73/AN3	R14	SMC_GPU_VSENSE	IN	53	
		P74/AN4	P14	SMC_DCIN_ISENSE	IN	50	
		P75/AN5	R15	SMC_PBUS_VSENSE	IN	50	
		P76/AN6	N13	SMC_BATT_ISENSE	IN	50	
		P77/AN7	P15	SMC_NB_1V25_ISENSE	IN	50	
		P80/PME*	C7	SMC_WAKE_SCI_L	OUT	13 25	
		P81/GA20	A7	SMC_P81		50	
		P82/CLKRUN*	B7	PM_CLKRUN_L	OUT	7 25 51	
		P83/LPCPD*	D6	PM_SUS_STAT_L	IN	7 25 50 51	
		P84/IRQ3*/TXD1	C6	SMC_TX_L	OUT	7 46 49 50 51	
		P85/IRQ4*/RXD1	A6	SMC_RX_L	IN	7 46 49 50 51	
		P86/IRQ5*/SCK1/SCL1	B6	(OC) SMB_MGMT_CLK	BI	52	
		P90/IRQ2*	K4	SMC_ONOFF_L	IN	50	
		P91/IRQ1*	J2	SMC_BC_ACOK	IN	50	
		P92/IRQ0*	J1	SMC_BS_ALRT_L	IN	50	
		P93/IRQ12*	J3	PM_SLP_S3_L_SMC			
		P94/IRQ13*	J4	PM_S4_STATE_L_SMC			
		P95/IRQ14*	H2	PM_SLP_S5_L	IN	25 50	
		P96/EXCL	H1	SMC_SUS_CLK	IN	50	
		P97/IRQ15*/SDA0	G2	(OC) SMB_0_S0_DATA	BI	52	

R4950 100 5% 1/16W MF-LF 402
PM_SLP_S3_L IN 6 7 25 70 75 78

R4951 100 5% 1/16W MF-LF 402
PM_S4_STATE_L IN 7 25 46 75 78

50 PP3V3_S5_AVREF_SMC
50 6 =PP3V3_S5_SMC

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/16W MF-LF 402
PP3V3_S5_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1
SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

OMIT
U4900
SMC_H8S2116
BGA
(3 OF 4)

		AVCC	N14	F2	VCC		
		AVCC	N15	F3	VCC		
				J15	VCC		
				A1	VCC		
				F1	VCL		
		AVREF	M14				
		AVREF	M15				
51 50 7	IN	SMC_RESET_L		E3	RES*		
50		SMC_XTAL		A2	XTAL		
50		SMC_EXTAL		B2	EXTAL		
		MD1	E2			SMC_MD1	IN 7 51
		MD2	K1			SMC_KBC_MDE	
		NMI	F4			SMC_NMI	IN 7 51
		ETRST*	L1			SMC_TRST_L	IN 7 51
			P12				
			R12				
		VSS	D1 P4 R4 F12 F13 B13 A13 A4 B4 D2				
		AVSS					

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402
NO STUFF

XW4900 SM

GND_SMC_AVSS 50 53 58

OMIT

(DEBUG_SW_1) 50 SMC_PA0
(DEBUG_SW_2) 50 SMC_PA1
28 25 7 OUT PM_SYSRST_L (OC)
46 OUT USB_DEBUGPRT_EN_L (OC)
31 16 BI PM_EXTTS_L<0> (OC)
32 16 BI PM_EXTTS_L<1> (OC)
50 BI SYS_ONEWIRE (OC)
25 OUT PM_BATLOW_L (OC)

		PA0/KIN8*/PA2DC	R3	PE0	M3	SMC_CASE_OPEN	IN 50
		PA1/KIN9*/PA2DD	P3	PE1*/ETCK	M2	SMC_TCK	IN 7 50 51
		PA2/KIN10*/PS2AC	R2	PE2*/ETDI	M1	SMC_TDI	IN 7 50 51
		PA3/KIN11*/PS2AD	N3	PE3*/ETDO	L4	SMC_TDO	OUT 7 50 51
		PA4/KIN12*/PS2BC	R1	PE4*/ETMS	L2	SMC_TMS	IN 7 50 51
		PA5/KIN13*/PS2BD	N2	PF0/IRQ8*/PWM2	M7	SMC_PF0	50
		PA6/KIN14*/PS2CC	M4	PF1/IRQ9*/PWM3	P6	SMC_PF1	50
		PA7/KIN15*/PS2CD	N1	PF2/IRQ10*/TMOY	R6	SMC_LID	IN 50
				PF3/IRQ11*/TMOX	N6	SMC_PF3	50
(DEBUG_SW_3) 50 SMC_PB0		PB0/LSMI*	R10	PF4/PWM4	M6	SMC_BATT_ISET	OUT 50
25 OUT SMC_RUNTIME_SCI_L		PB1/LSCI	A10	PF5/PWM5	R5	SMC_BATT_VSET	OUT 50
50 IN SMC_ODD_DETECT		PB2	D10	PF6/PWM6	P5	SMC_SYS_ISET	OUT 50
53 50 OUT ISENSE_CAL_EN		PB3	A11	PF7/PWM7	N5	SMC_SYS_VSET	OUT 50
50 IN SMC_EXCARD_CP		PB4	B11				
50 OUT SMC_EXCARD_PWR_EN		PB5	C11	PG0/EXIRQ8*/TMIX	P9	SMC_PG0	50
50 IN SMC_EXCARD_OC_L		PB6	A12	PG1/EXIRQ9*/TMIY	R9	=SMC_SMS_INT	IN 50
85 IN SMC_GFX_OVERTEMP_L		PB7	D11	PG2/EXIRQ10*/SDA2	N9	(OC) SMB_BSA_DATA	BI 52
56 OUT SMC_FAN_0_CTL		PC0/TIOCA0/WUE8*	G14	PG3/EXIRQ11*/SCL2	P8	(OC) SMB_BSA_CLK	BI 52
56 OUT SMC_FAN_1_CTL		PC1/TIOCB0/WUE9*	G15	PG4/EXIRQ12*/EXSDAA	R8	(OC) SMB_A_S3_DATA	BI 52
57 OUT SMC_FAN_2_CTL		PC2/TIOCC0/TCLKA/WUE10*	G13	PG5/EXIRQ13*/EXSCLA	M8	(OC) SMB_A_S3_CLK	BI 52
50 OUT SMC_FAN_3_CTL		PC3/TIOCD0/TCLKB/WUE11*	G12	PG6/EXIRQ14*/EXSDAB	P7	(OC) SMB_B_S0_DATA	BI 52
56 IN SMC_FAN_0_TACH		PC4/TIOCA1/WUE12*	H14	PG7/EXIRQ15*/EXSCLB	R7	(OC) SMB_B_S0_CLK	BI 52
56 IN SMC_FAN_1_TACH		PC5/TIOCB1/TCLKC/WUE13*	H15				
57 IN SMC_FAN_2_TACH		PC6/TIOCA2/WUE14*	H13	PH0/EXIRQ6*	E1	SMC_PROCHOT	OUT 50
50 IN SMC_FAN_3_TACH		PC7/TIOCB2/TCLKD/WUE15*	H12	PH1/EXIRQ7*	F3	SMC_THRMTRIP	OUT 50
				PH2/FWE	K2	SMC_FWE	IN 50
108 50 IN SMS_X_AXIS		PD0/AN8	M11	PH3/EXEXCL	C4	ALS_GAIN	OUT 50
108 50 IN SMS_Y_AXIS		PD1/AN9	P11	PH4	D4	SMC_PH4	50
108 50 IN SMS_Z_AXIS		PD2/AN10	N11	PH5	B3	SMS_ONOFF_L	OUT 50
50 IN SMC_ANALOG_ID		PD3/AN11	N11				
50 IN SMC_NB_CORE_ISENSE		PD4/AN12	P10				
50 IN SMC_NB_1V8_ISENSE		PD5/AN13	N10				
50 IN ALS_LEFT		PD6/AN14	N10				
58 IN ALS_RIGHT		PD7/AN15	M10				

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

OMIT
U4900
SMC_H8S2116
BGA
(4 OF 4)

NC	G3	NC0		NC12	F15	NC	
NC	H3	NC1		NC13	A14	NC	
NC	F3	NC2		NC14	C12	NC	
NC	L3	NC3		NC15	C10	NC	
NC	N4	NC4		NC16	C5	NC	
NC	M5	NC5		NC17	A3	NC	
NC	N7	NC6		NC18	B8	NC	
NC	M12	NC7		NC19	E4	NC	
NC	M13	NC8		NC20	H4	NC	
NC	L12	NC9		NC21	M9	NC	
NC	K15	NC10		NC22	N8	NC	
NC	J14	NC11					

PRELIMINARY

SMC

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=12/15/2006

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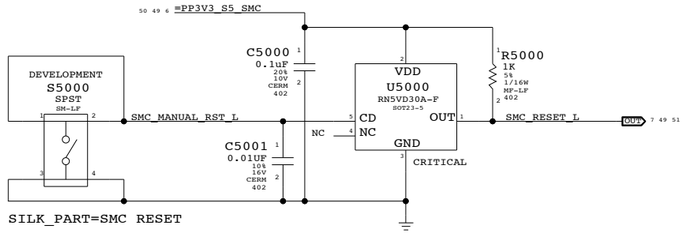
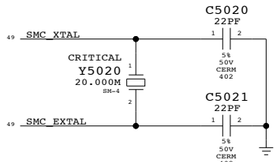
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 49 OF 118	

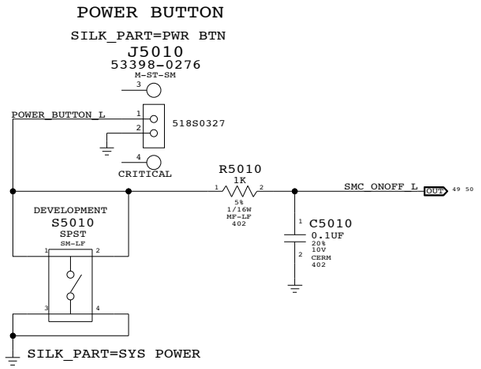
SMC Reset Button / Brownout Detect



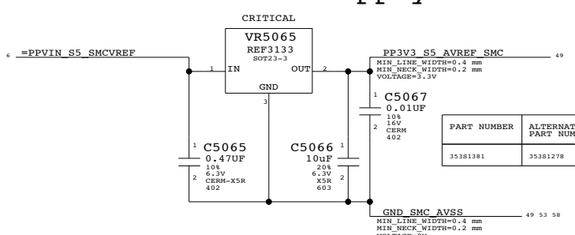
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



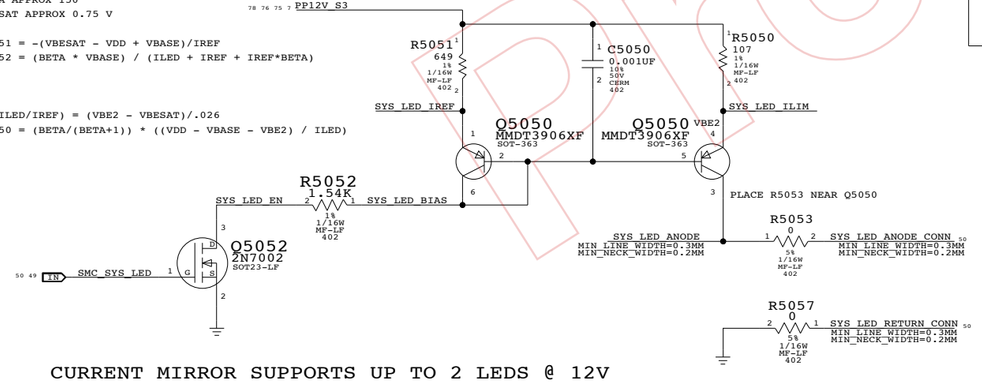
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Intersil ISL60002-33

SYSTEM (SLEEP) LED CIRCUITS

ILED = 20 MA
IREF = 5 MA @ 12V
VBASE = VFMAX LED = 4V*2 = 8
BETA APPROX 150
VBESAT APPROX 0.75 V

R5051 = -(VBESAT - VDD + VBASE)/IREF
R5052 = (BETA * VBASE) / (ILED + IREF + IREF*BETA)

LN(ILED/IREF) = (VBE2 - VBESAT)/.026
R5050 = (BETA/(BETA+1)) * ((VDD - VBASE - VBE2) / ILED)



CURRENT MIRROR SUPPORTS UP TO 2 LEDS @ 12V
BOOST CIRCUIT UP TO 3 LEDS ON LGP

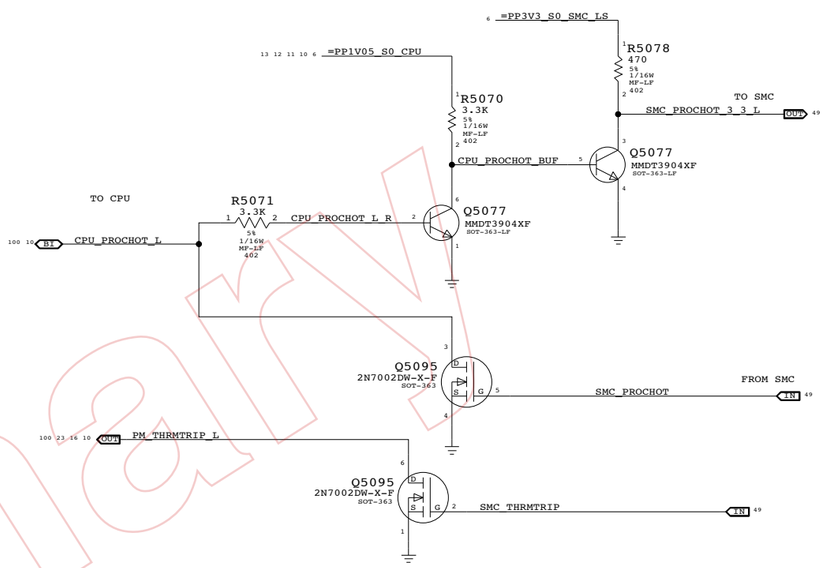
UNUSED TP/NC ALIASES

SMC_BATT_ISET	NC_SMC_BATT_ISET	NO_TEST=TRUE	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	NO_TEST=TRUE	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	NO_TEST=TRUE	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	NO_TEST=TRUE	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	NO_TEST=TRUE	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	NO_TEST=TRUE	MAKE_BASE=TRUE
SMS_X_AXIS	NC_SMS_X_AXIS	NO_TEST=TRUE	MAKE_BASE=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	NO_TEST=TRUE	MAKE_BASE=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	NO_TEST=TRUE	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN		MAKE_BASE=TRUE
ALS_LEFT	TP_ALS_LEFT		MAKE_BASE=TRUE
SMC_P14	TP_SMC_P14		MAKE_BASE=TRUE
SMC_P20	TP_SMC_P20		MAKE_BASE=TRUE
SMC_P21	TP_SMC_P21		MAKE_BASE=TRUE
SMC_P22	TP_SMC_P22		MAKE_BASE=TRUE
SMC_P23	TP_SMC_P23		MAKE_BASE=TRUE
SMC_P26	TP_SMC_P26		MAKE_BASE=TRUE
SMC_P27	TP_SMC_P27		MAKE_BASE=TRUE
SMC_P43	TP_SMC_P43		MAKE_BASE=TRUE
SMC_P44	TP_SMC_P44		MAKE_BASE=TRUE
SMC_P45	TP_SMC_P45		MAKE_BASE=TRUE
SMC_P62	TP_SMC_P62		MAKE_BASE=TRUE
SMC_P63	TP_SMC_P63		MAKE_BASE=TRUE
SMC_P64	TP_SMC_P64		MAKE_BASE=TRUE
SMC_P81	TP_SMC_P81		MAKE_BASE=TRUE
SMC_PF0	TP_SMC_PF0		MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1		MAKE_BASE=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL		MAKE_BASE=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH		MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN		MAKE_BASE=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN		MAKE_BASE=TRUE
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED		MAKE_BASE=TRUE
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN		MAKE_BASE=TRUE
SMC_RSTGATE_L	TP_SMC_RSTGATE_L		MAKE_BASE=TRUE
SMS_ONOFF_L	TP_SMS_ONOFF_L		MAKE_BASE=TRUE
SMC_P46	TP_SMC_P46		MAKE_BASE=TRUE

UNUSED SENSORS

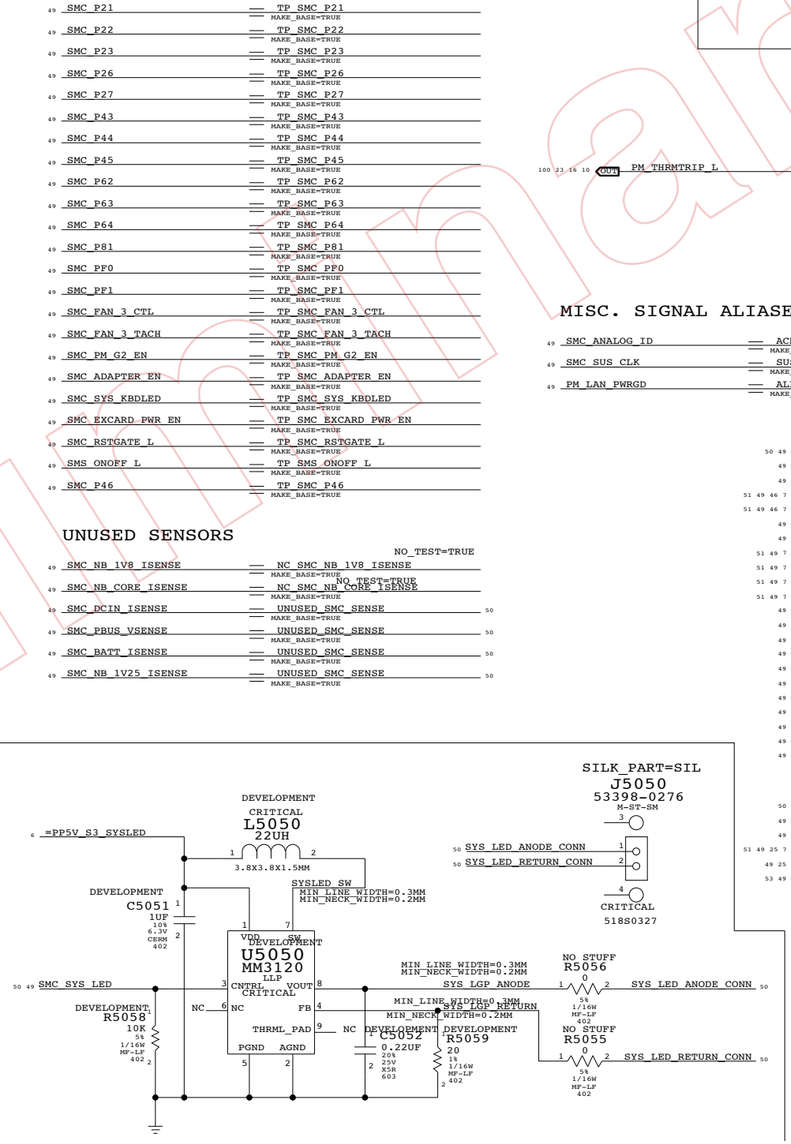
SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE	NO_TEST=TRUE
SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE	NO_TEST=TRUE
SMC_DCIN_ISENSE	UNUSED_SMC_SENSE	
SMC_PBUS_VSENSE	UNUSED_SMC_SENSE	
SMC_BATT_ISENSE	UNUSED_SMC_SENSE	
SMC_NB_1V25_ISENSE	UNUSED_SMC_SENSE	

SMC FSB to 3.3V Level Shifting



MISC. SIGNAL ALIASES

SMC_ANALOG_ID	ACDC_TEMP	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE
PM_LAN_PWRGD	ALL_SYS_PWRGD	MAKE_BASE=TRUE



SMC Support

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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=PP3V3_S5_SMC

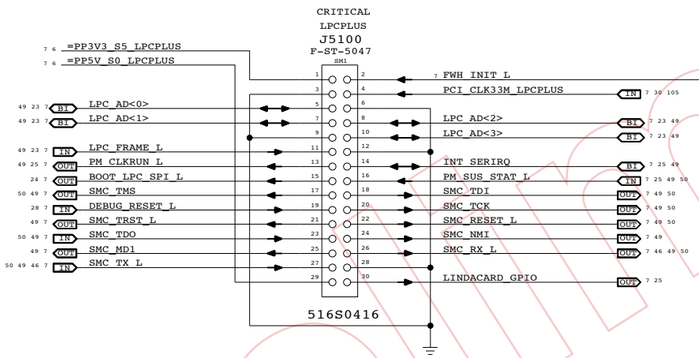
SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402	
SMC_LID	R5033	100K	5%	1/16W	MF-LF	402	
SMC_FWE	R5034	10K	5%	1/16W	MF-LF	402	
SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402	
SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402	
SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402	
SMC_BS_ALRT_L	R5038	100K	5%	1/16W	MF-LF	402	
SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402	
SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402	
SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402	
SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402	
SMC_EXCARD_OC_L	R5043	10K	5%	1/16W	MF-LF	402	
SMC_PF3	R5080	10K	5%	1/16W	MF-LF	402	
SMC_PH4	R5082	10K	5%	1/16W	MF-LF	402	
SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402	
SMC_ODD_DETECT	R5087	10K	5%	1/16W	MF-LF	402	
SMC_PA0	R5096	10K	5%	1/16W	MF-LF	402	
SMC_PA1	R5090	10K	5%	1/16W	MF-LF	402	
SMC_PB0	R5091	10K	5%	1/16W	MF-LF	402	
=SMC_SMS_INT — SMC_SMS_INT	R5092	10K	5%	1/16W	MF-LF	402	
SMC_P67	R5093	10K	5%	1/16W	MF-LF	402	
SMC_PG0	R5094	10K	5%	1/16W	MF-LF	402	

UNUSED_SMC_SENSE	R5086	10K	5%	1/16W	MF-LF	402	
SMC_CASE_OPEN	R5046	10K	5%	1/16W	MF-LF	402	
SMC_EXCARD_CP	R5048	10K	5%	1/16W	MF-LF	402	
PM_SUS_STAT_L	R5083	100K	5%	1/16W	MF-LF	402	
PM_SLP_S5_L	R5084	100K	5%	1/16W	MF-LF	402	
ISENSE_CAL_EN	R5088	100K	5%	1/16W	MF-LF	402	NO STUFF

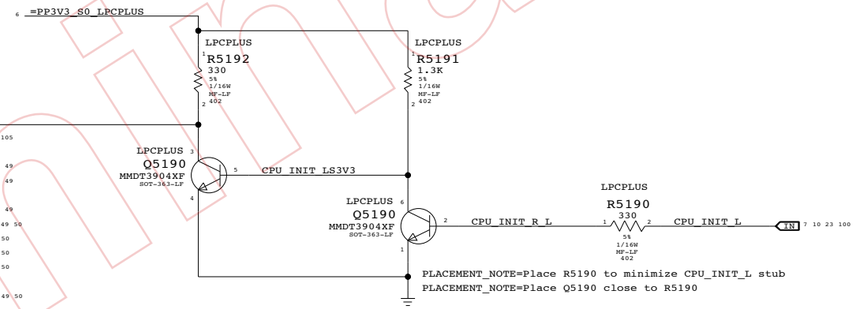
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7228	REV. 27	
	SCALE NONE	SHT 50	OF 118	

Preliminary

LPC+ Connector



FWH_INIT_L Generation



Preliminary

LPC+ Debug Connector

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=03/22/2007

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APPLE COMPUTER INC.

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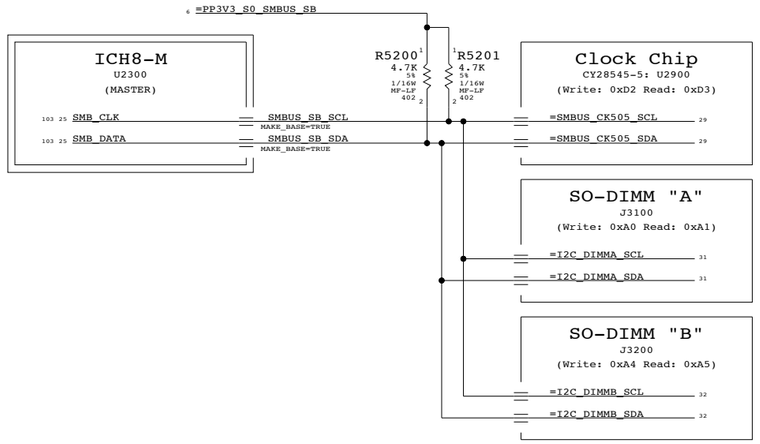
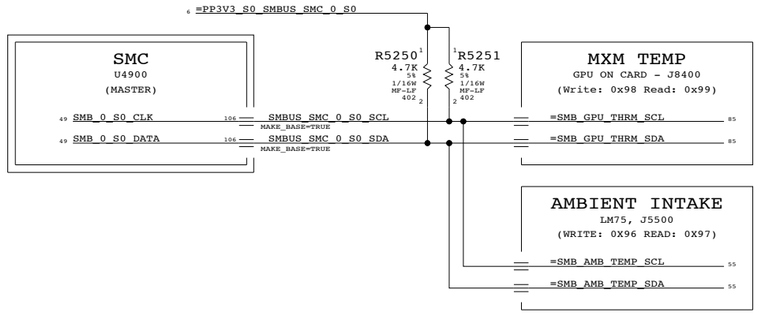
D	051-7228	27
SCALE: NONE	SHT 51 OF 118	

ICH8-M SMBus Connections

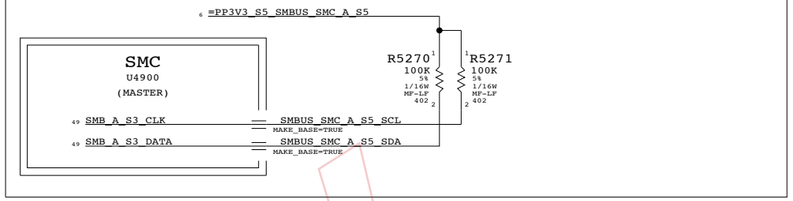


SMC "0" SMBus Connections

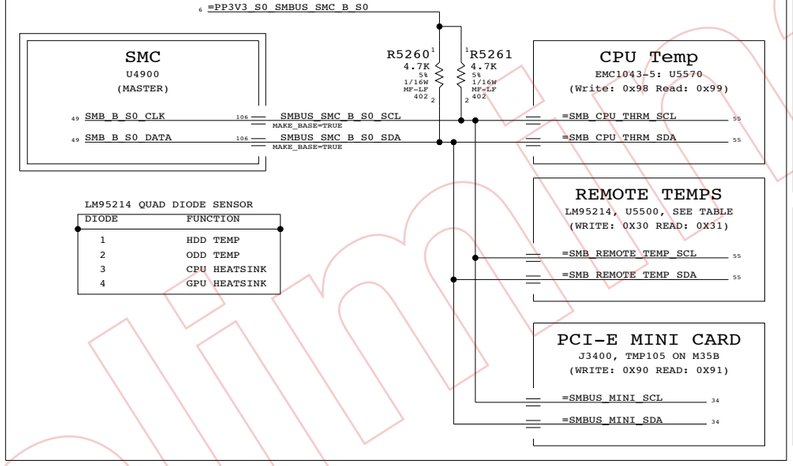


SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S5 STATE



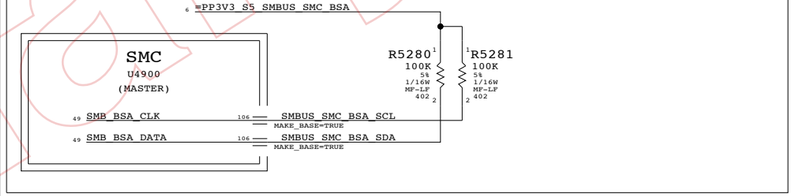
SMC "B" SMBus Connections



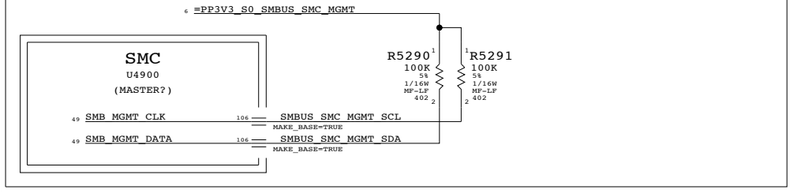
LM95214 QUAD DIODE SENSOR

DIODE	FUNCTION
1	HDD TEMP
2	ODD TEMP
3	CPU HEATSINK
4	GPU HEATSINK

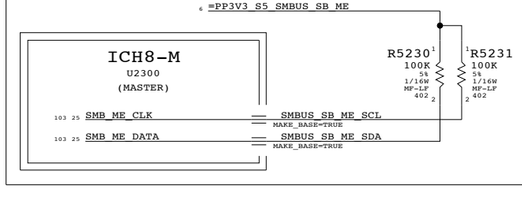
UNUSED SMC "BATTERY A" SMBUS CONNECTIONS



UNUSED SMC "MANAGEMENT" SMBUS CONNECTIONS



UNUSED ICH8-M ME SMBUS CONNECTIONS



SMBUS CONNECTIONS

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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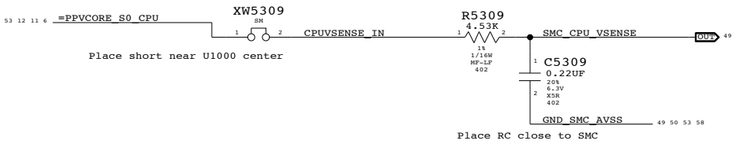
SCALE: NONE	SHT 52 OF 118	

Preliminary

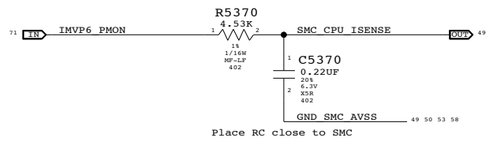
CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Voltage Sense / Filter



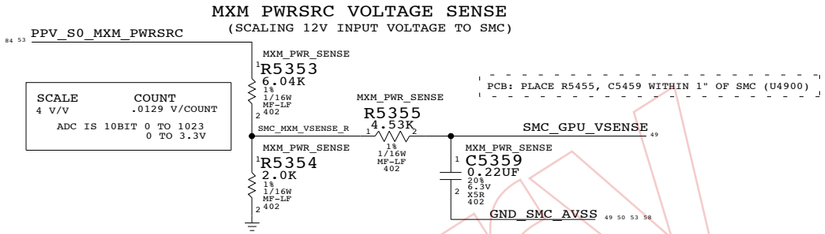
CPU SUPPLY POWER SENSE FILTER



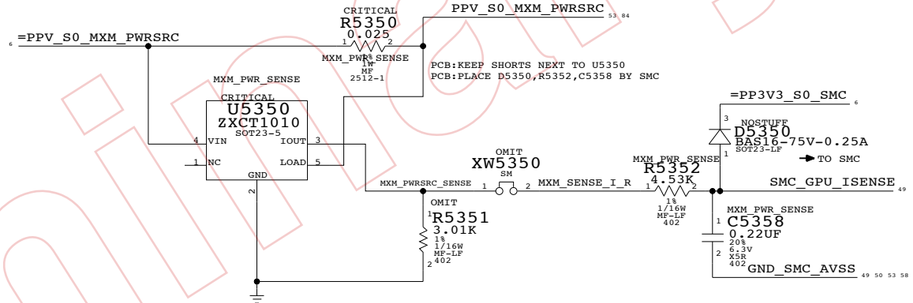
PCPU = VPMON / (17.5 * .0021)

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



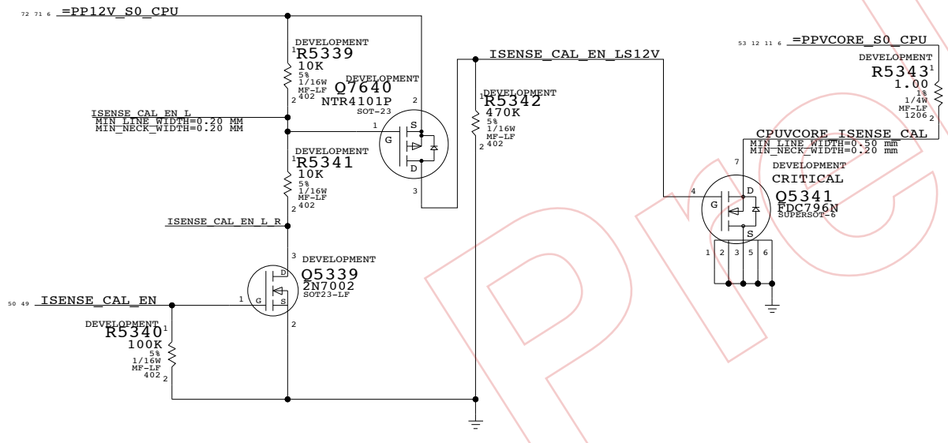
M78 SET FOR APPROX 3V AT 5A ON PWRSRC
MXM-HE CAN GO TO 16A, BUT M78
CARDS TARGET MAX 55W AT 12V

SCALE	COUNT
1.6461 A/V	.005309969 A/COUNT
ADC IS 10BIT	0 TO 1023
	0 TO 3.3V

M72 SET FOR APPROX 3V AT 4A ON PWRSRC

SCALE	COUNT
1.3289 A/V	.004286786 A/COUNT
ADC IS 10BIT	0 TO 1023
	0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0264	1	RES,3.01K,1%,402	R5351	20_INCH_LCD
114S0254	1	RES,2.43K,1%,402	R5351	24_INCH_LCD



Current & Voltage Sensing

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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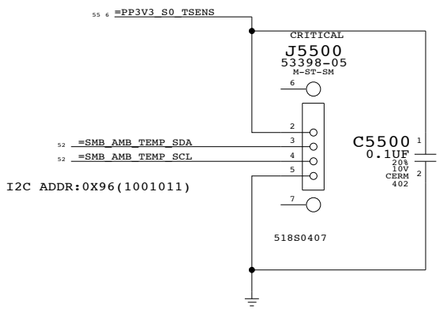
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 53 OF 118	

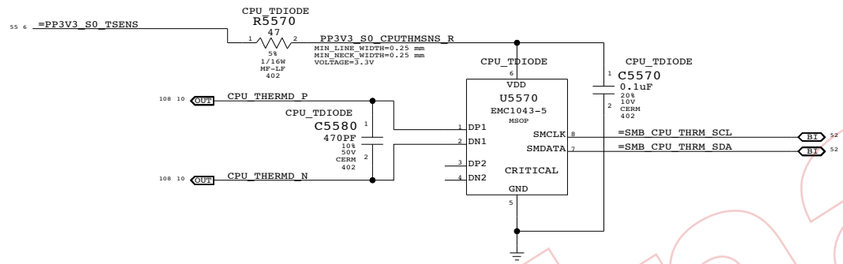
Preliminary

REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

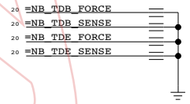
AMBIENT TEMP SENSOR



CPU T-Diode Thermal Sensor

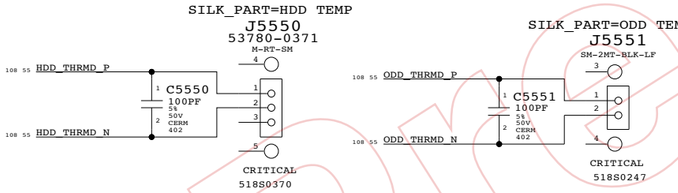


UNUSED NB THERMAL SENSORS

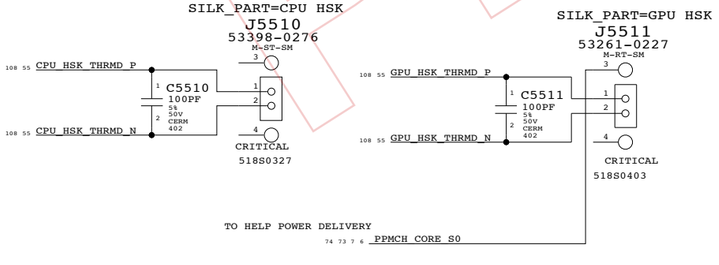


PLACE ALL CAPS NEAR U5500

PLACE DISK SENSOR CONNS BOTTOM SIDE

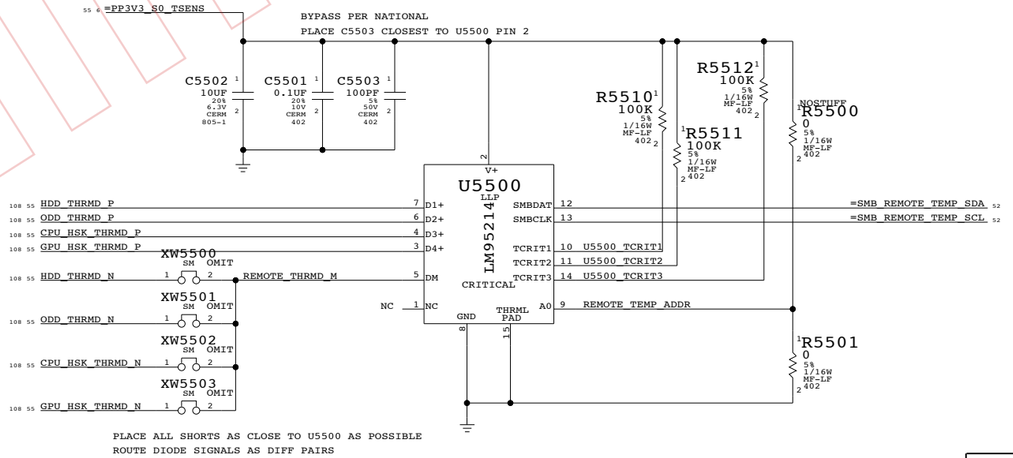


PLACE HSK SENSOR CONN. TOP SIDE NEAR GPU OR CPU



TO HELP POWER DELIVERY

74 73 7 6 PPMCH_CORE_S0



Thermal Sensors

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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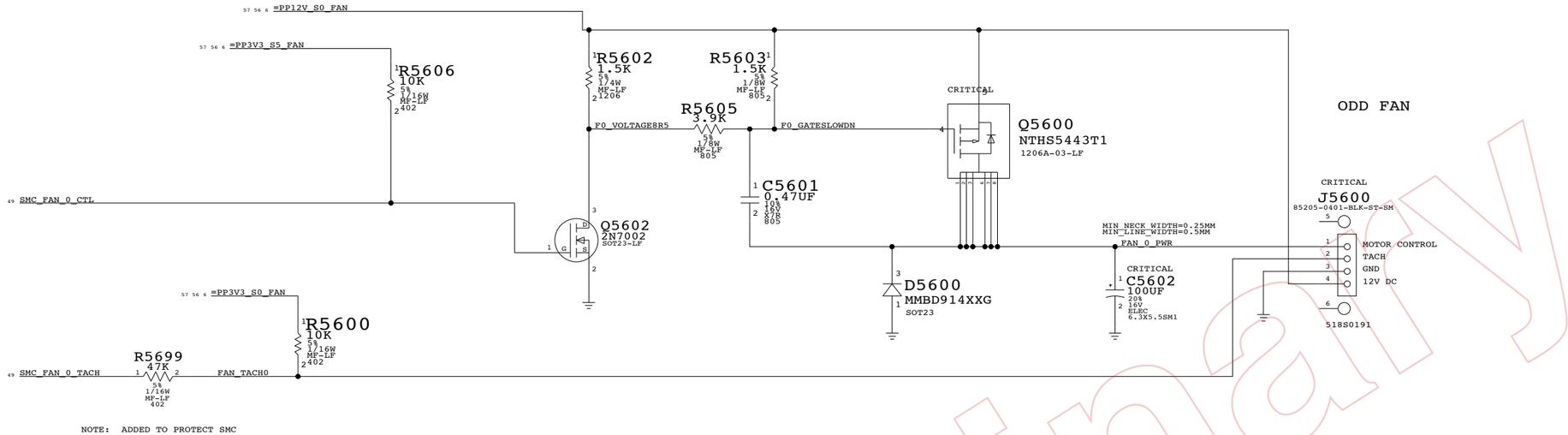
SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
NONE	55	118

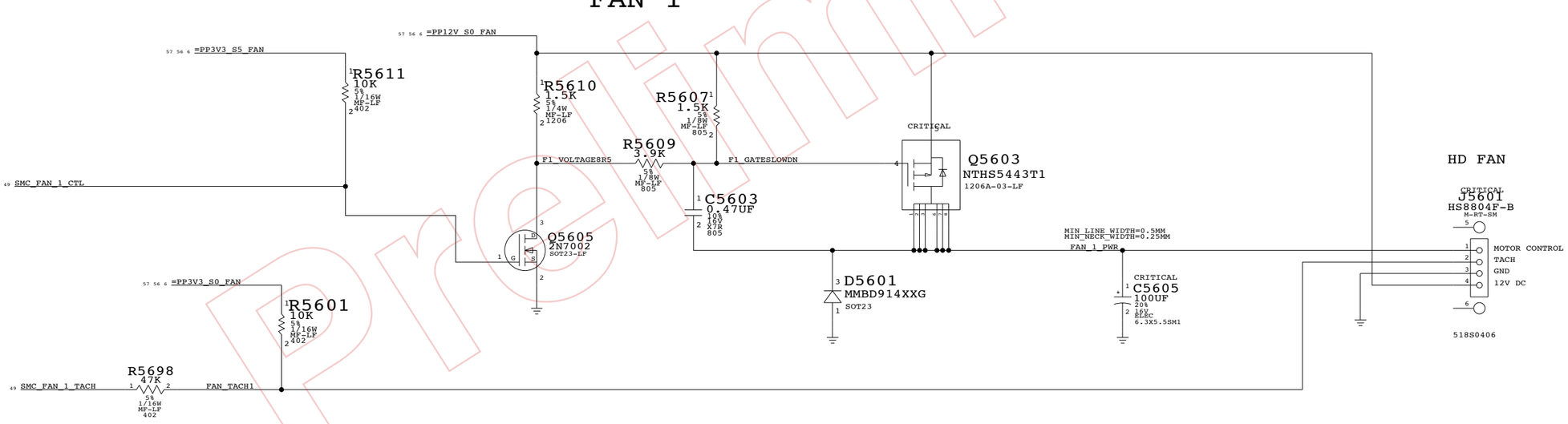
Preliminary

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



Preliminary

HD AND OD FAN

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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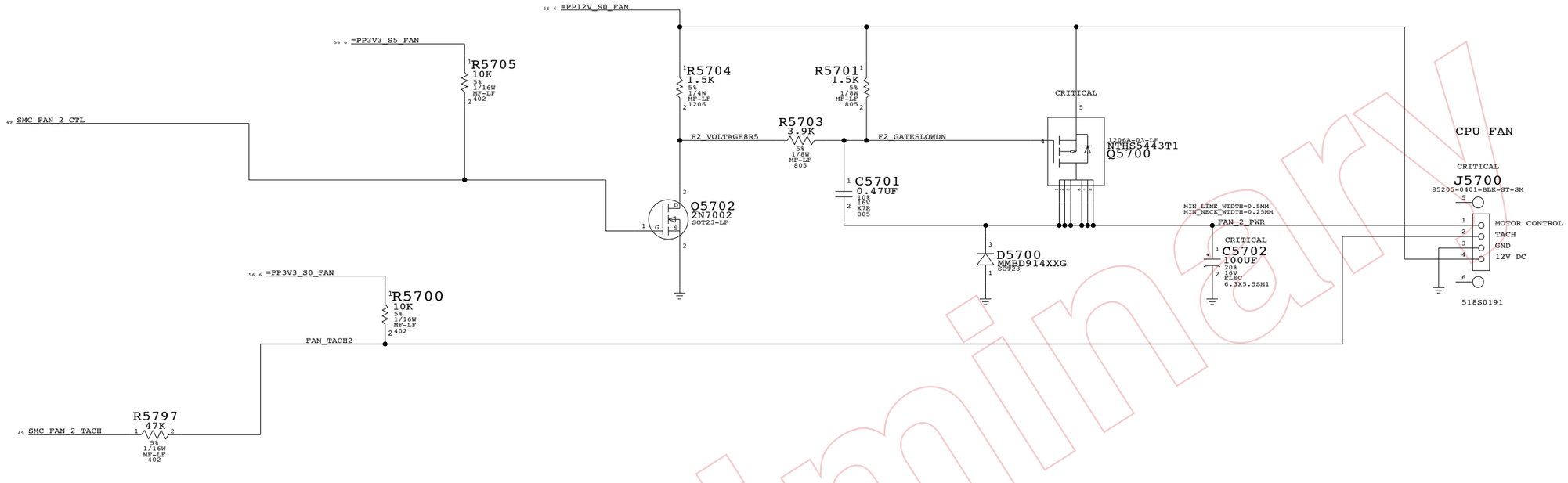
SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE: NONE SHT 56 OF 118

FAN 2



Preliminary

CPU FAN

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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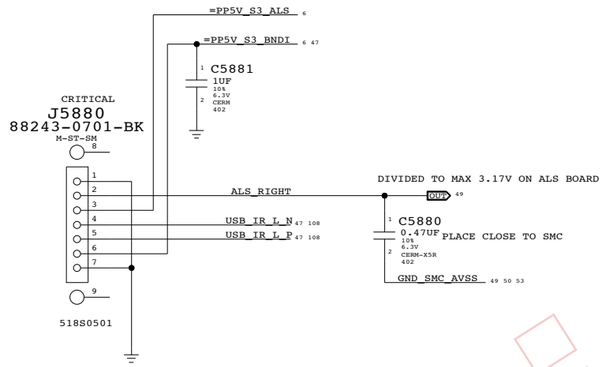
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 57 OF 118	

ANALOG ALS & IR



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ALS Support

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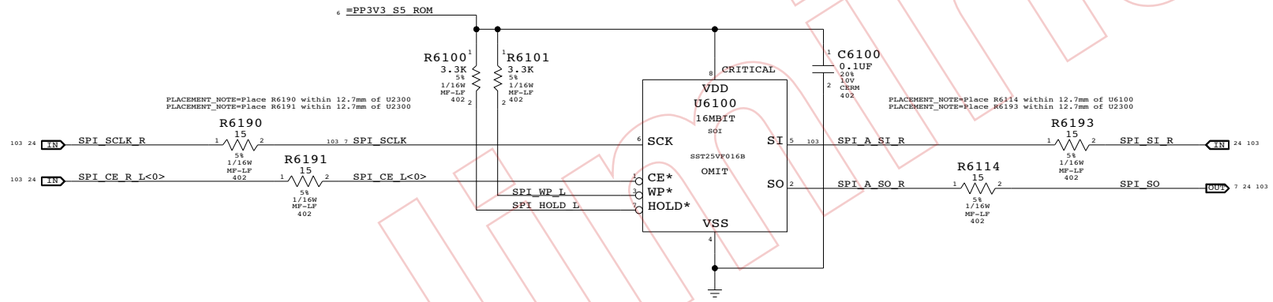
SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
NONE	58	118



Preliminary

SPI BootROM

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=03/22/2007

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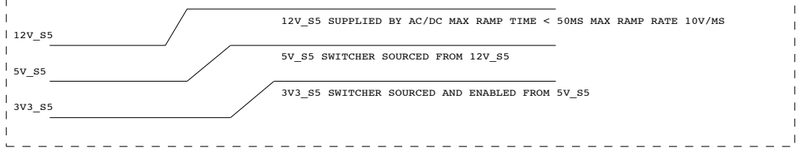
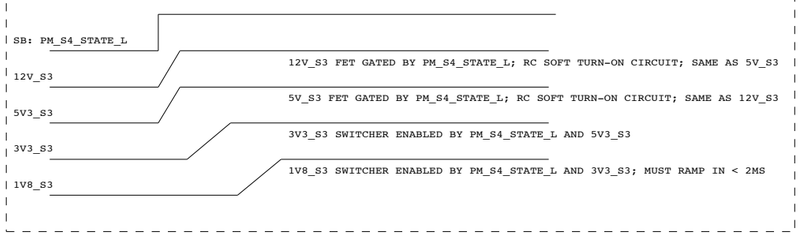
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 61 OF 118	

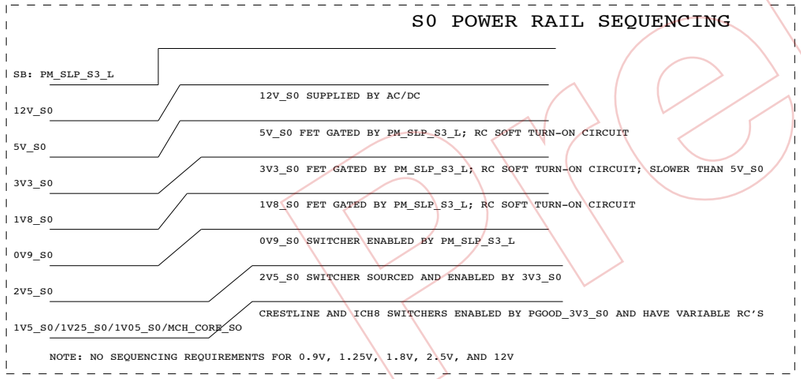
S5 POWER RAIL SEQUENCING



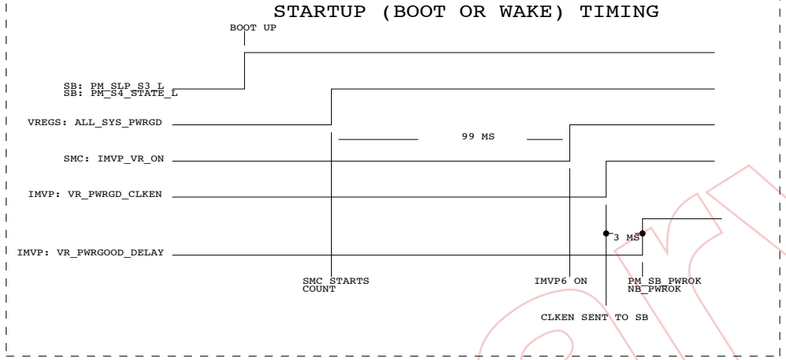
S3 POWER RAIL SEQUENCING



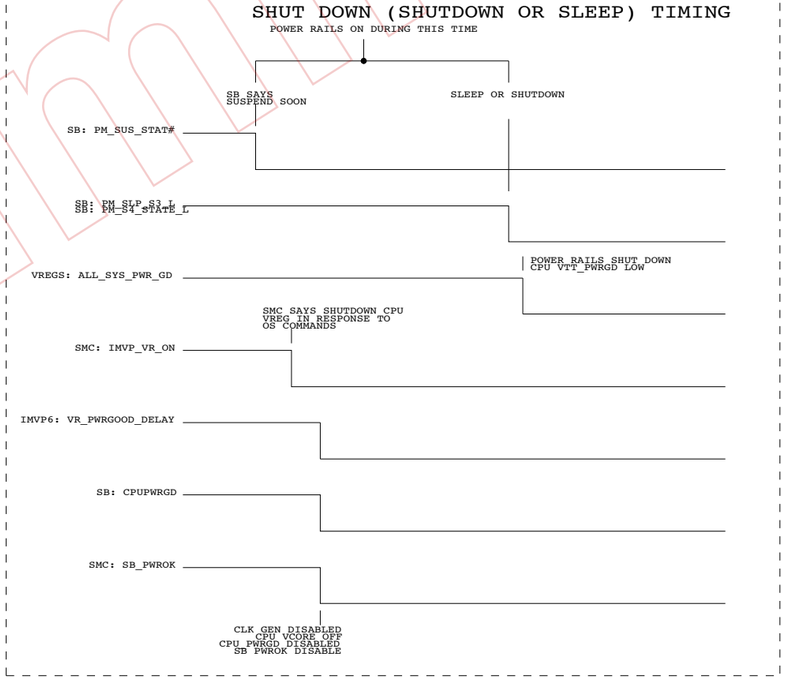
S0 POWER RAIL SEQUENCING



STARTUP (BOOT OR WAKE) TIMING



SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



Preliminary

POWER SEQUENCING BLOCK DIAGRAM

SYNC_MASTER=MARK SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
NONE	69	118

PGOOD Comparators

PP12V_S5 — C7010 0.1UF 20% 16V CERM 603

PP5V_S5 — R7010 2.21K 1% 1/16W MF-LF 402 — R7013 7.5K 1% 1/16W MF-LF 402 — R7018 5.62K 1% 1/16W MF-LF 402 — R7020 1.62K 1% 1/16W MF-LF 402

PP3V3_S0 — R7000 2.74K 1% 1/16W MF-LF 402

PP1V8_S0 — R7001 1.43K 1% 1/16W MF-LF 402

PP5V_S0 — R7002 3.92K 1% 1/16W MF-LF 402

PP0V9_S0 — R7003 715 1% 1/16W MF-LF 402

R7011 1K 1% 1/16W MF-LF 402 — R7014 10K 1% 1/16W MF-LF 402 — R7019 1K 1% 1/16W MF-LF 402 — R7021 10K 1% 1/16W MF-LF 402

(2.94V/2.61V; 330MV HYSTERESIS)
(1.58V/1.41V; 172MV HYSTERESIS)
(4.47V/4.00V; 470MV HYSTERESIS)
(0.76V/0.67V; 85MV HYSTERESIS)

U7010 LM339A SOI-LF

-1	5VS5_2V80_REF	4
+1	3V3S0_COMP_REF	5
-2	5VS5_1V53_REF	6
+2	1V8S0_COMP_REF	7
-3	5VS5_4V24_REF1	8
+3	5VS0_COMP_REF	9
-4	5VS5_0V76_REF	10
+4	0V9S0_COMP_REF	11
	GND	12
	OUT1	2
	OUT2	1
	OUT3	14
	OUT4	13

R7005 100K 1% 1/16W MF-LF 402 — R7006 100K 1% 1/16W MF-LF 402 — R7007 100K 1% 1/16W MF-LF 402 — R7008 100K 1% 1/16W MF-LF 402

PGOOD_3V3_S0 OUT 70 77
PGOOD_1V8_S0 OUT 70
PGOOD_5V_S0 OUT 70
PGOOD_0V9_S0 OUT 70

NOSTUFF C7000 0.1uF 20% 10V CERM 402
NOSTUFF C7001 0.1uF 20% 10V CERM 402
NOSTUFF C7002 0.1uF 20% 10V CERM 402
NOSTUFF C7003 0.1uF 20% 10V CERM 402

(PULLUPS ARE NEAR LOADS)

(HYSTERESIS)
(R7000: 16.5K; R7001: 17.4K; R7002: 24.9K; R7003: 8.25K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)
(R7010: 21.5K; R7011: 7.15K; R7018: 52.3K; R7020: 1.37K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)

1.05V/MCH_CORE S0 RUN/SS CONTROL

PP3V3_S5 — R7070 5.1K 5% 1/16W MF-LF 402

PGOOD_3V3_S0 (IN) — R7040 0 5% 1/16W MF-LF 402 — PGOOD_CR_S0 — R7065 100K 5% 1/16W MF-LF 402 — 1V05S0_RUNSS_BUF — R7066 330 5% 1/16W MF-LF 402 — 1V05S0_RUNSS (OUT) 73 74

PGOOD_12V_S0 (IN) — R7041 0 5% 1/16W MF-LF 402

Q7007 SSM6N15FE SOT563 — RUNSS_GATE_D_L

C7062 0.01UF 10% 16V CERM 402

1.25V S0 RUN/SS CONTROL

R7063 51K 5% 1/16W MF-LF 402 — 1V25S0_RUNSS_BUF — R7064 680 5% 1/16W MF-LF 402 — 1V25S0_RUNSS (OUT) 74

Q7006 SSM6N15FE SOT563 — RUNSS_GATE_D_L

C7061 0.01UF 10% 16V CERM 402

1.5V S0 RUN/SS CONTROL

R7061 10K 5% 1/16W MF-LF 402 — 1V5S0_RUNSS_BUF — R7062 1K 5% 1/16W MF-LF 402 — 1V5S0_RUNSS (OUT) 73

PP5V_S5 — R7060 470K 5% 1/16W MF-LF 402

CRITICAL Q7007 SSM6N15FE SOT563 — RUNSS_GATE_D_L

C7060 0.01UF 10% 16V CERM 402

CRITICAL Q7006 SSM6N15FE SOT563

PM_SLP_S3_L (IN) 78 75 49 25 7 6

(SUPPLY CHANGED FOR ROUTING)

PP5V_S3 — (REMOVE AFTER DEVELOPMENT, MAKE INTO TP) — R7080 100K 5% 1/16W MF-LF 402 — PP3V3_S3

PGOOD_1V8_S3 (IN) 75

R7081 100K 5% 1/16W MF-LF 402

PGOOD_3V3_S3 (IN) 76

PWROK Sequencing

PP3V3_S0 — R7034 5.1K 5% 1/16W MF-LF 402

(MC74VHC1G08 HAS 100NS/V MAX SLEW RATE) (10PF MAX CIN)

PP3V3_S5 — C7052 0.1uF 20% 10V CERM 402 — C7056 0.1uF 20% 10V CERM 402

U7052 MC74VHC1G08 SOT23-5-LF

PGOOD_0V9_S0 (IN) — R7030 100 5% 1/16W MF-LF 402 — PGOOD_S0_OUT1

PGOOD_5V_S0 (IN) — R7031 100 5% 1/16W MF-LF 402

PGOOD_1V8_S0 (IN) — R7032 100 5% 1/16W MF-LF 402

PGOOD_2V5_S0 (IN) — R7033 100 5% 1/16W MF-LF 402

NVIDIA

ALL_SYS_PWRGD (OUT) 7 49 50 84

VR_PWRGOOD_DELAY (IN) 71 22 16 7

U7056 MC74VHC1G08 SOT23-5-LF

PM_SB_PWROK (OUT) 7 25 28

(NOT ALL PGOODS ARE NEEDED HERE SINCE SOME REGULATORS ARE DAISY CHAIN ENABLED)

PP3V3_S0 — R7039 5.1K 5% 1/16W MF-LF 402

PGOOD_MCH_CORE_S0 (IN) — R7035 100 5% 1/16W MF-LF 402 — IMVP_PGD_IN

PGOOD_1V05_S0 (IN) — R7036 100 5% 1/16W MF-LF 402

PGOOD_1V25_S0 (IN) — R7037 100 5% 1/16W MF-LF 402

PGOOD_1V5_S0 (IN) — R7038 100 5% 1/16W MF-LF 402

PP3V3_S5 — R7092 10K 5% 1/16W MF-LF 402

(3.3V WILL NOT BE UP UNTIL 5V IS IN REGULATION)
(SMC CAN HANDLE SLOW RISE TIME OF RSMRST_PWRGD)

PGOOD_3V3_S5 (IN) 77 — RSMRST_PWRGD MAKE_BASE=TRUE (OUT) 49

NOSTUFF C7090 220PF 5% 25V CERM 402

Preliminary

PGOOD and Power Sequencing

SYNC_MASTER=MARK SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT: 70	OF: 118

IMVP6 CPU VCORE REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0330	1	RES,MTL FILM,1/16W,14.7K,1,0402,SMD,LF	R7116		HIGH_TDP
114S0324	1	RES,MTL FILM,1/16W,12.7K,1,0402,SMD,LF	R7116		LOW_TDP

TO SUPPORT LOW TDP MEROM AND HIGH TDP MEROM ON SAME BOARD:

- 35W TDP: 55A CONTINUOUS CURRENT
  SET R7116 TO 12.7K; OC TRIP POINT OF 60.5A
- 55W TDP: 64A CONTINUOUS CURRENT
  SET R7116 TO 14.7K; OC TRIP POINT OF 70.0A

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

IMVP6_OCSET — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_VSUM — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_VO — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_FB — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_VW — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM
IMVP6_FCCM — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.20 MM — 1864

IMVP6_PWM1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.23 MM — 1849
IMVP6_PHASE1 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_UGATE1 — MIN_LINE_WIDTH=0.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_LGATE1 — MIN_LINE_WIDTH=0.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.23 MM
IMVP6_FET_RC1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_VSUM1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT1_RC — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM — 1863

IMVP6_PWM2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.23 MM — 1850
IMVP6_PHASE2 — MIN_LINE_WIDTH=1.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_UGATE2 — MIN_LINE_WIDTH=0.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_LGATE2 — MIN_LINE_WIDTH=0.5 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.23 MM
IMVP6_FET_RC2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_VSUM2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2 — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT2_RC — MIN_LINE_WIDTH=0.25 MM — MIN_NECK_WIDTH=0.25 MM — 1866

IMVP6 CPU VCore Regulator	
SYNC_MASTER=MARK	SYNC_DATE=N/A

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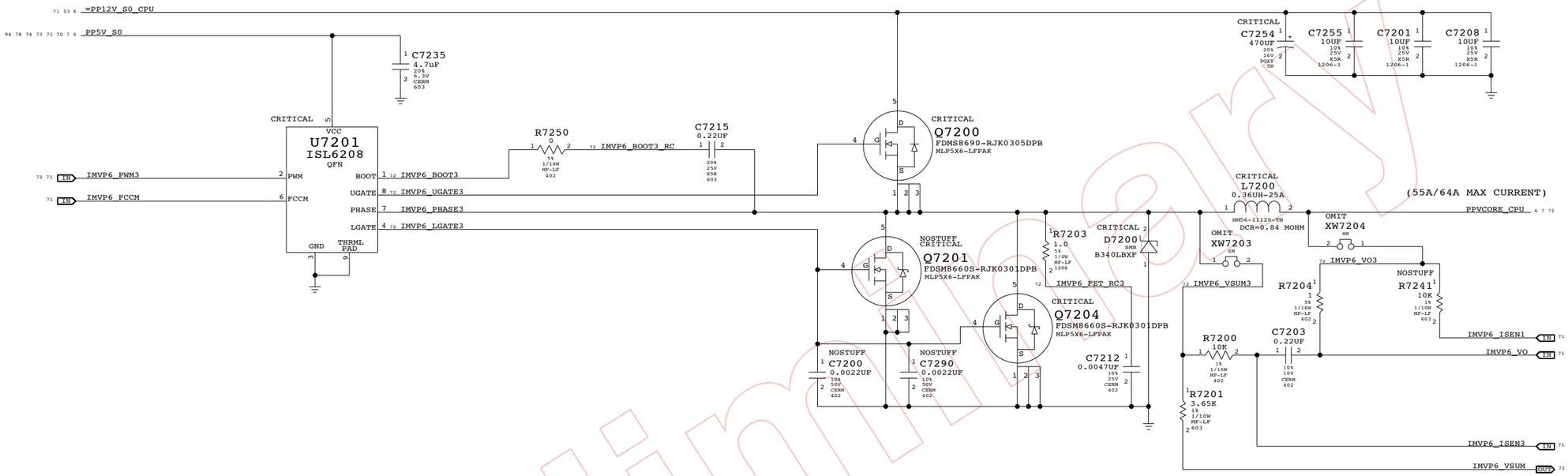
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 71 OF 118	

IMVP6 CPU VCORE REGULATOR



72 71	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	151
108 72	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	143
72	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	144
72	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	145
72	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	146
72 71	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	148
72	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	147
72	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72	IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	150
72	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	152

IMVP6 3RD PHASE

SYNC_MASTER=MARK SYNC_DATE=N/A

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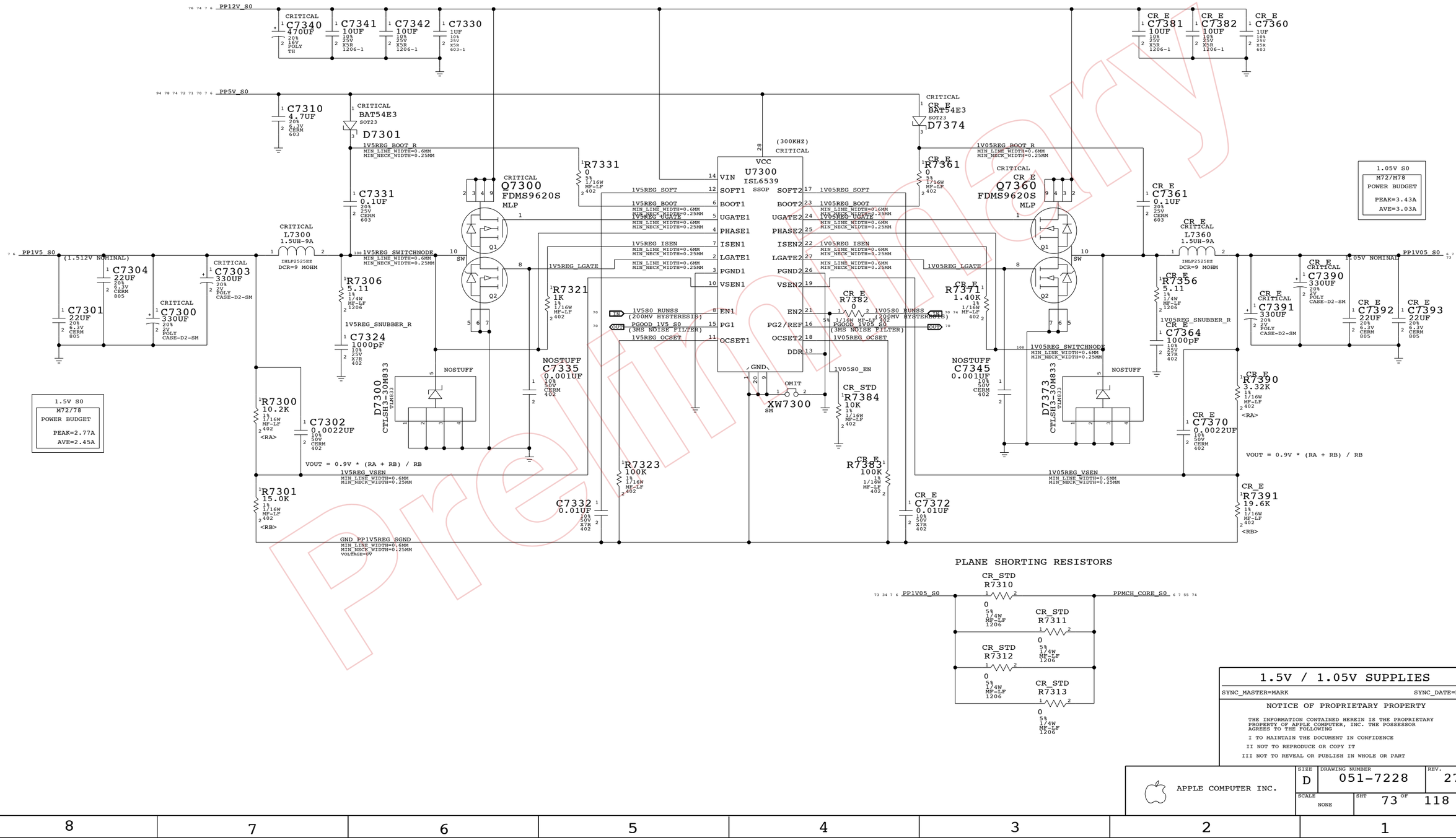
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 72 OF 118	

Preliminary

1.5V S0 & 1.05V SO RAILS



Preliminary

1.5V / 1.05V SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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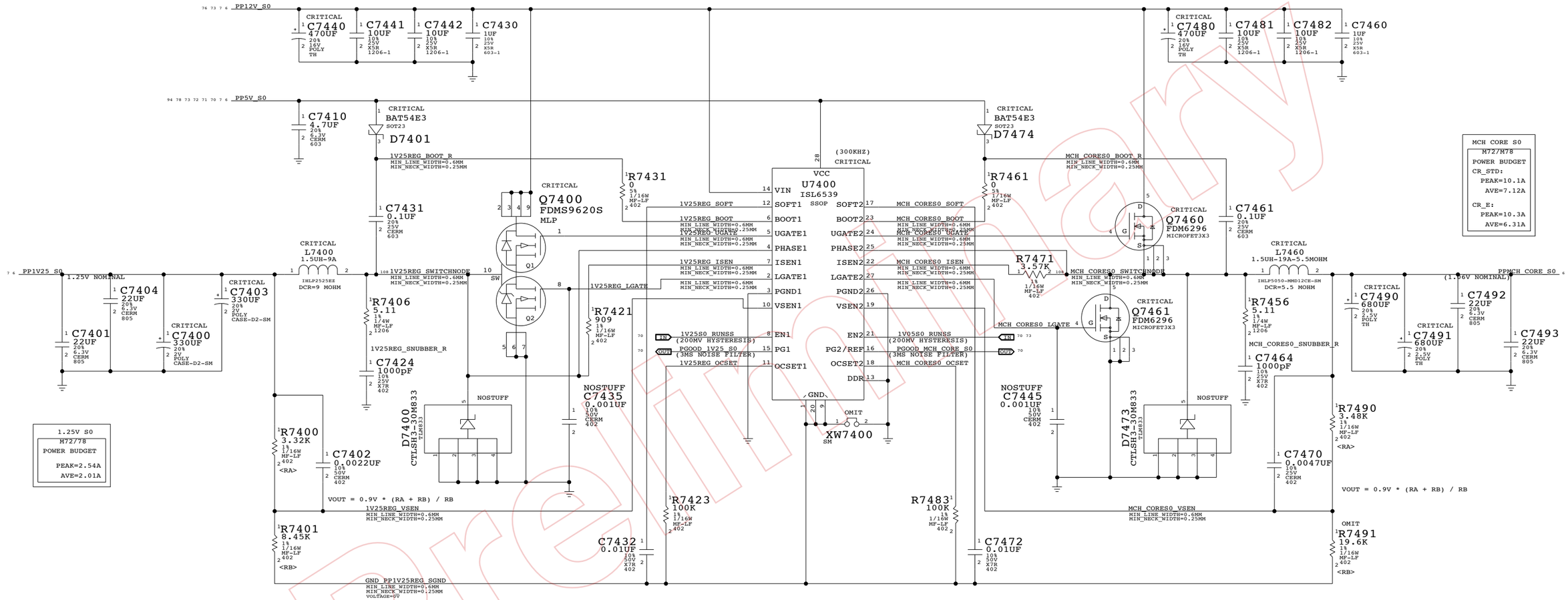
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 73 OF 118	

1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

Preliminary

1.25V / MCH CORE SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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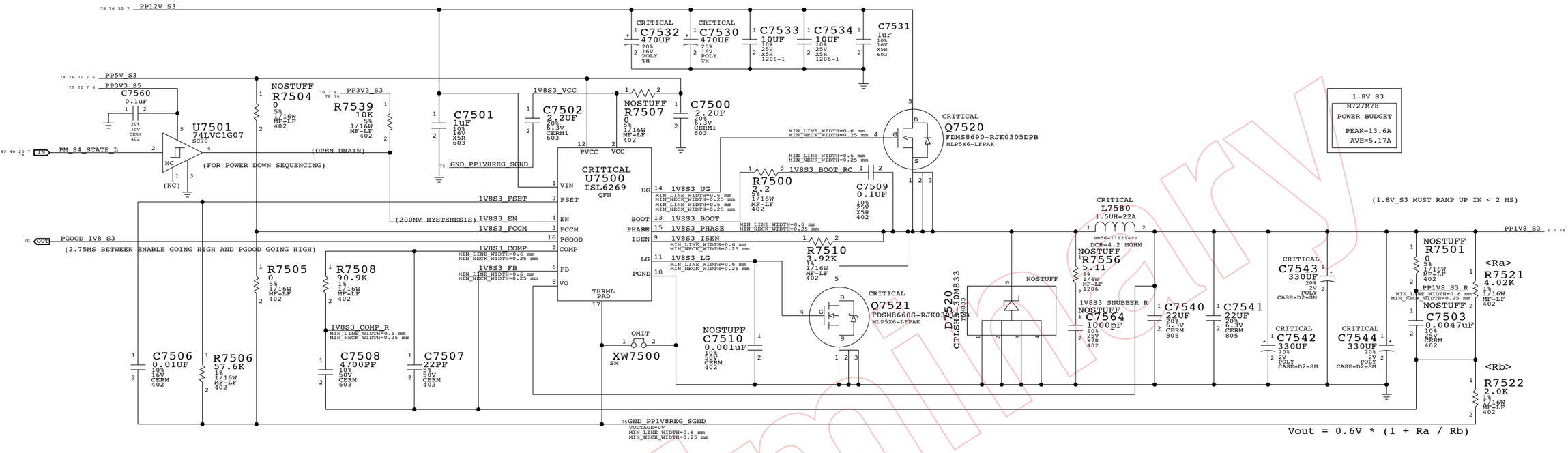
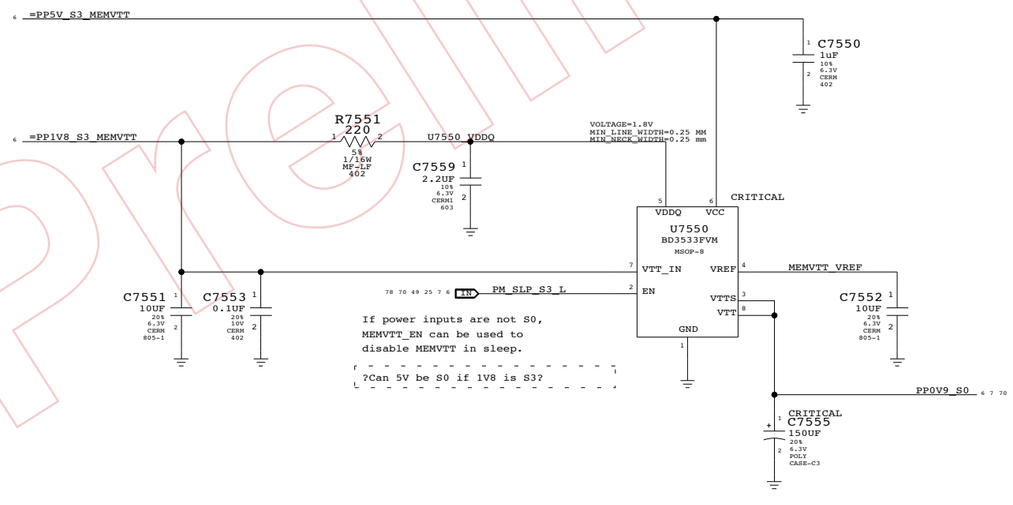
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 74 OF 118	

1.8V S3 / MEM VTT RAILS



DDR2 Vtt Regulator



1.8V S3 /0.9V S0 SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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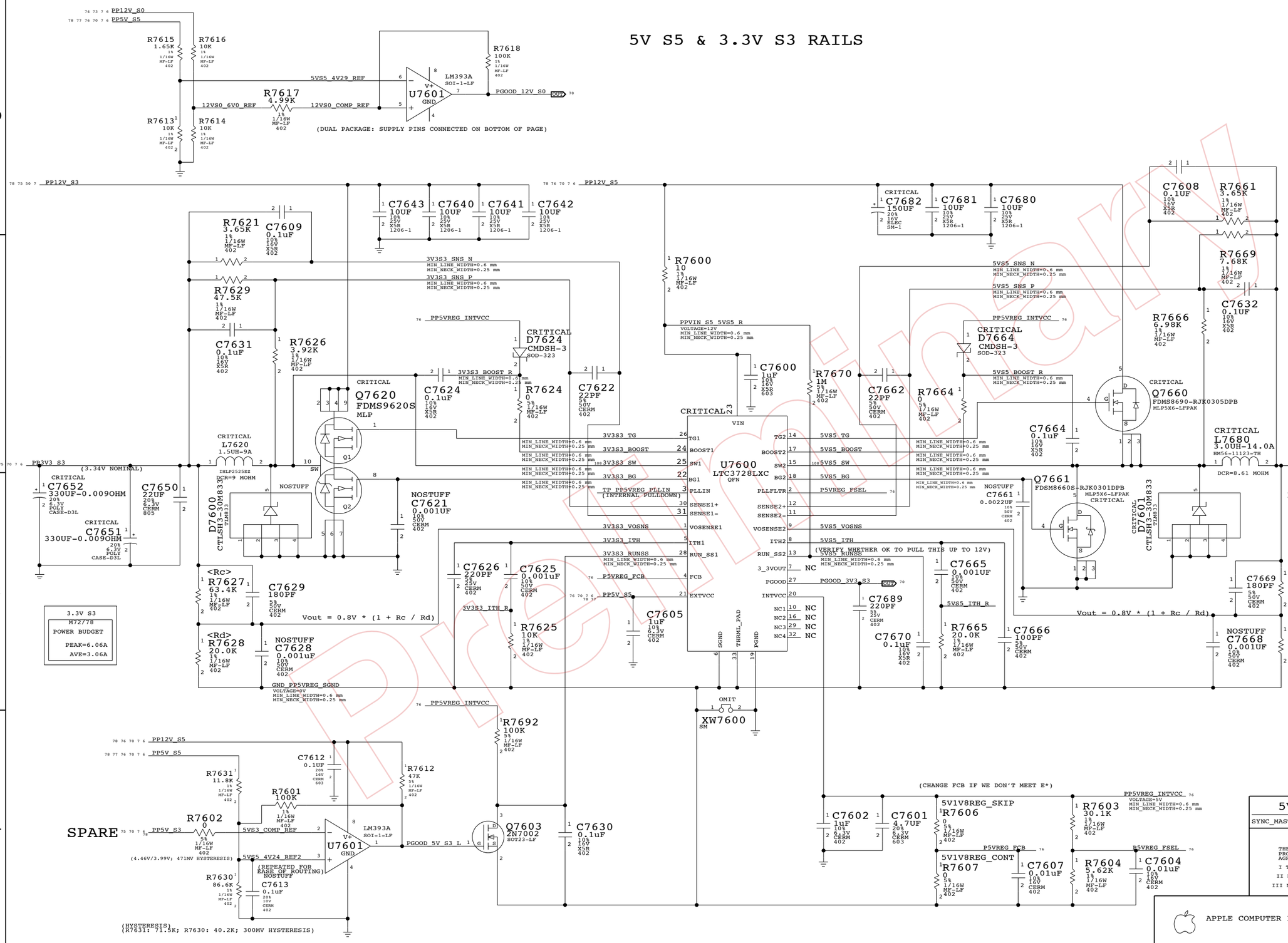
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 75 OF 118	

Preliminary

5V S5 & 3.3V S3 RAILS



5V S5 / 3.3V S3 SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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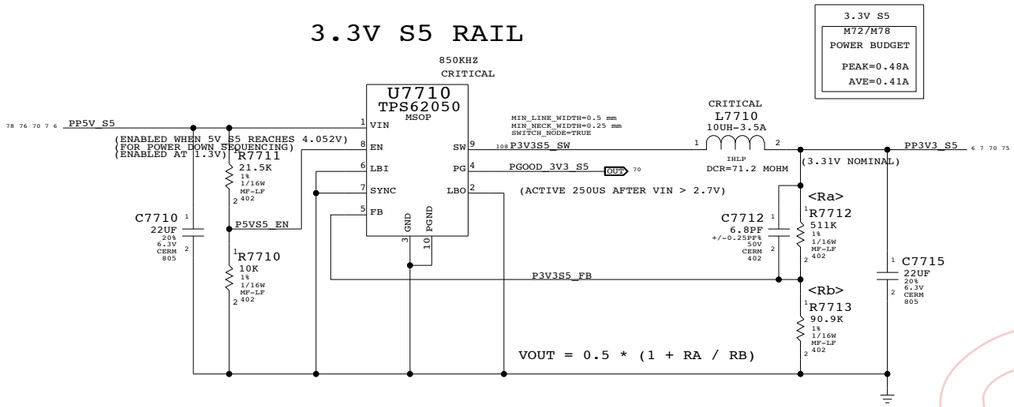
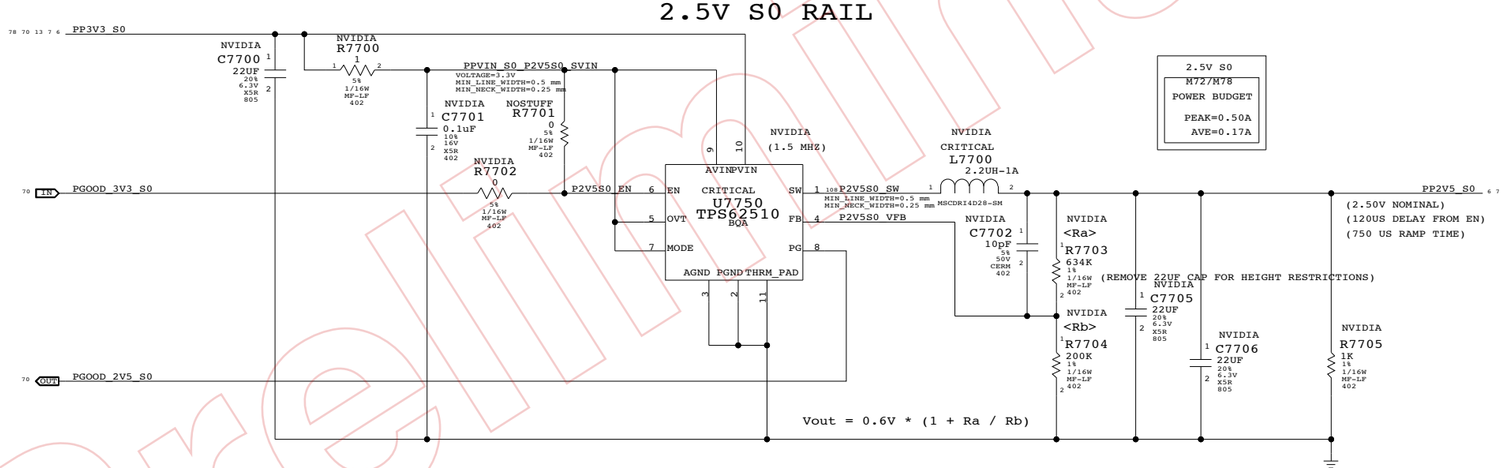
SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 76 OF 118	

3.3V S5 RAIL



2.5V S0 RAIL



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

3.3V / 2.5V POWER SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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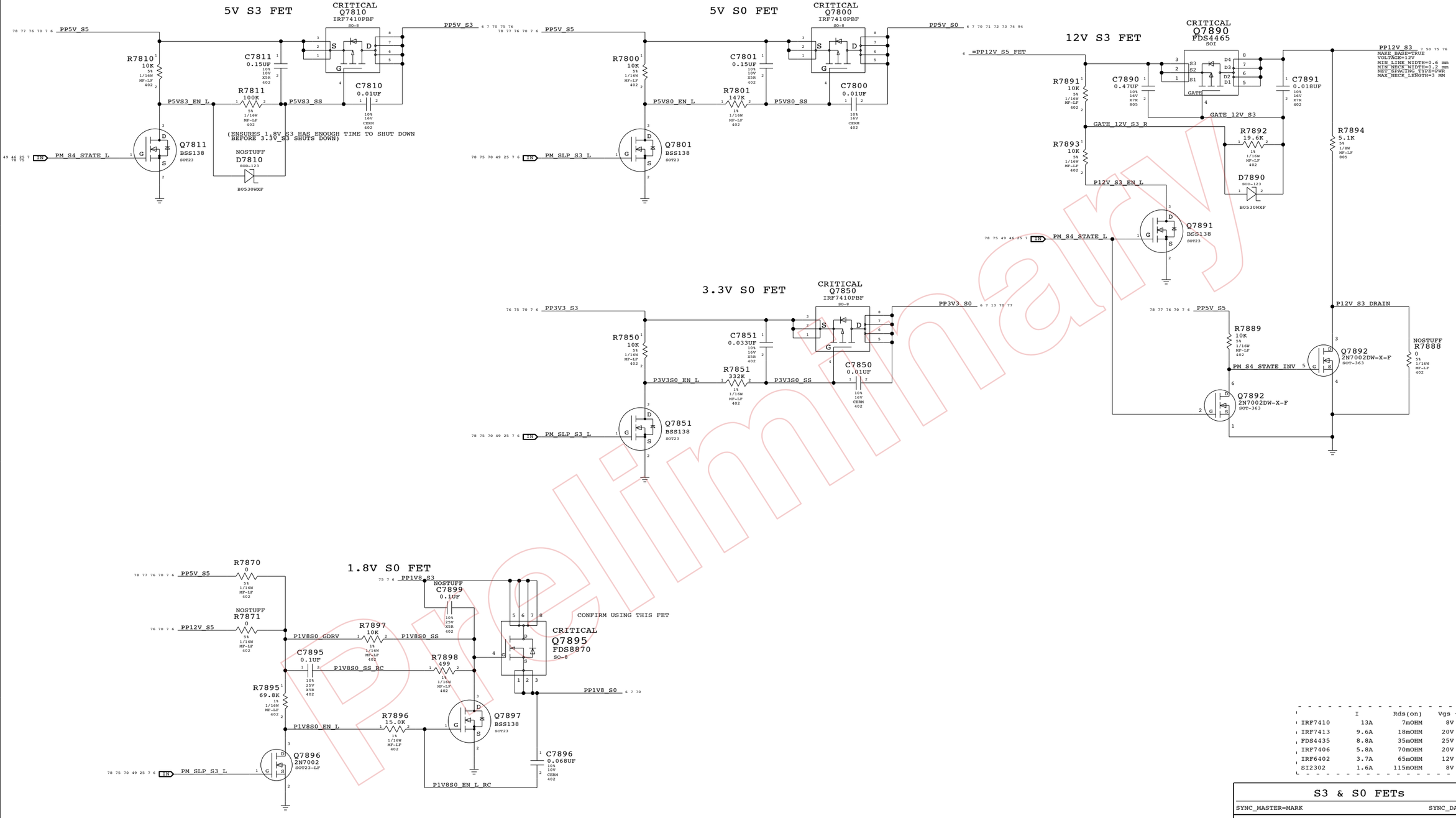
SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE: NONE SHT 77 OF 118

Preliminary



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=MARK SYNC_DATE=N/A

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D	051-7228	27
SCALE: NONE	SHT 78 OF 118	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

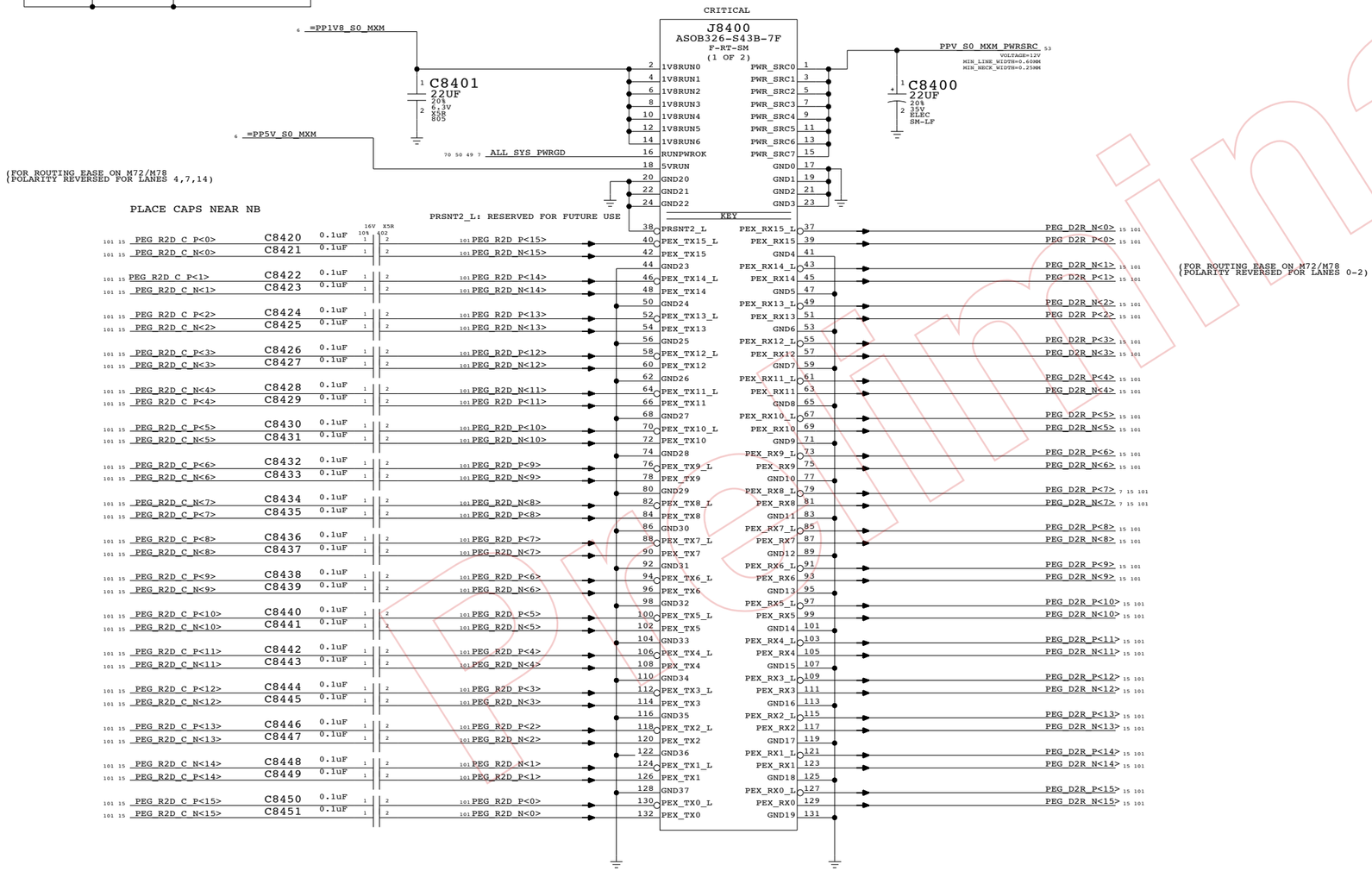
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



Preliminary

MXM PCI-E & PWR

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
24_INCH_LCD

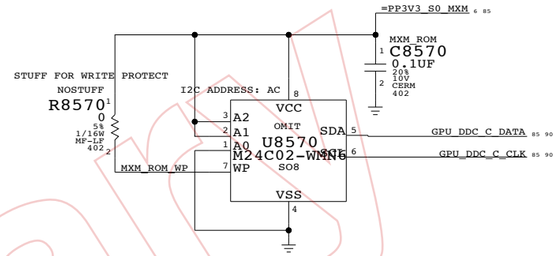
MXM SPEC POWER REQUIREMENTS

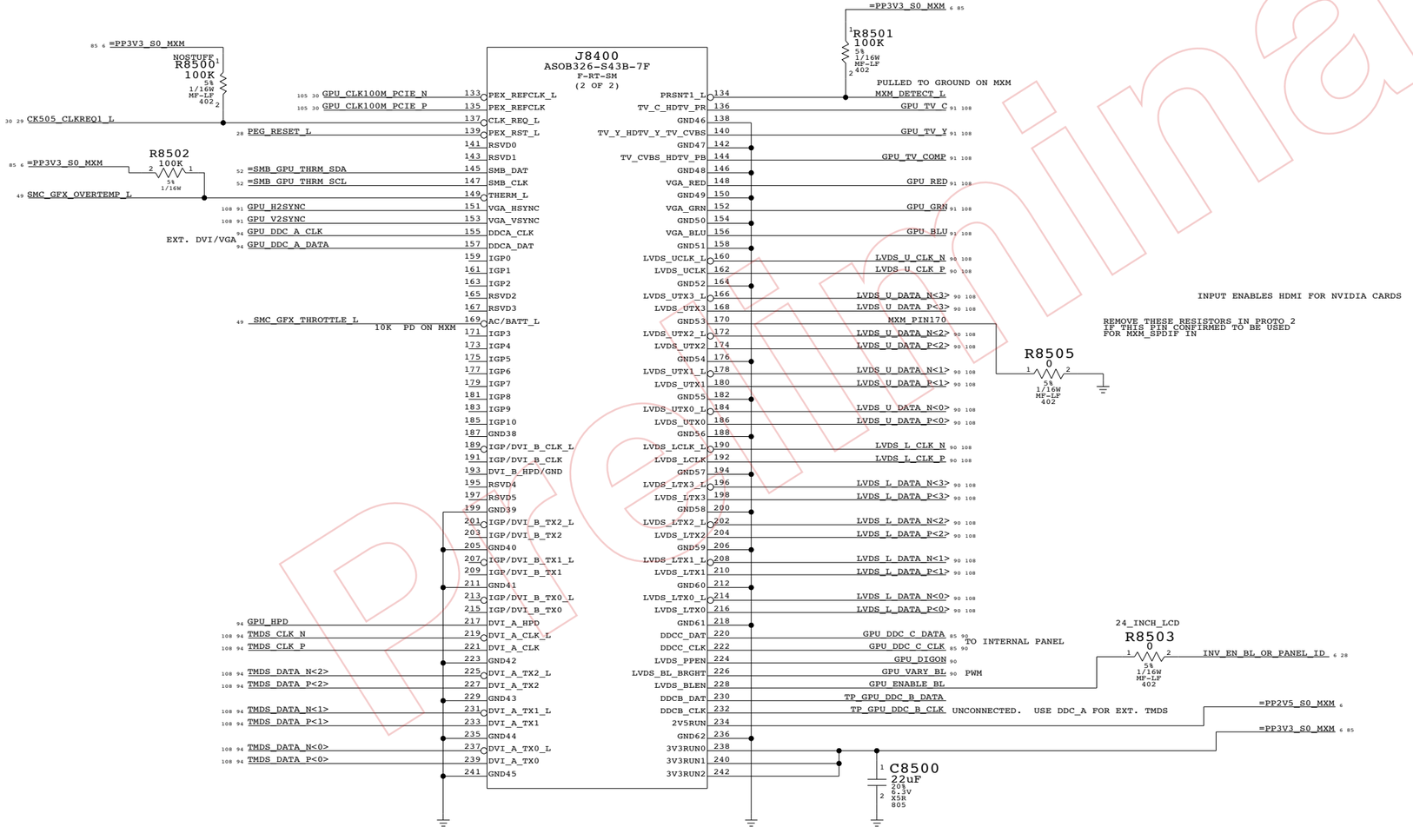
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400





MXM I/O

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Page Notes

Power aliases required by this page:
- =PPV_S0_LCD_24INCH
- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
20_INCH_LCD, 24_INCH_LCD

94 91 6 =PP3V3_S0_VIDEO — I20 — =PP3V3_DDC_LCD 90

LCD (LVDS) INTERFACE

24_INCH_LCD
R9002 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_24INCH 1 2

20_INCH_LCD
R9003 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_20INCH 1 2

PANEL POWER SEQUENCING

PPV_S0_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C9000 0.1UF 10% 50V X7R 603-1
PLACE NEAR J9002

NOSTUFF
R9090 0 5% 1/8W MF-LF 805

R9000 100K 5% 1/16W MF-LF 402
R9001 29.4K 1% 1/16W MF-LF 402
LCD_PWREN_DIV
LCD_PWREN_L_RC

Q9000 SI3443DV TSOP-LF
S G D

PPV_LCD_SW
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9000 FERR-250-OHM SM
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C9020 10UF 10% 16V X5R-CERM 1210
C9001 0.001uF 20% 50V CERM 402

PPV_LCD_CONN 6 90
5V FOR 20 INCH LCD
12V FOR 24 INCH LCD

OMIT
R9099 100K 5% 1/16W MF-LF 402
LCD_PWREN_L

Q9001 2N7002 SOT23-LF
85 GPU_DIGON
R9070 100K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	RES,100K,5%,0402	R9099		24_INCH_LCD
116S0004	1	RES,0,5%,0402	R9099		20_INCH_LCD

CRITICAL
SDF9000
STDOFF-3MMOD4.6MMH-1.35-TH

516S0241
CRITICAL
J9002
53307-3072
F-ST-SM

108 85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85 108
108 85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85 108
108 85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85 108
	7	8	LVDS_U_CLK_N 85 108
108 85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85 108
108 85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85 108
108 85 LVDS_L_DATA_P<0>	13	14	
108 85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85 108
	17	18	LVDS_L_DATA_N<2> 85 108
108 85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85 108
108 85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85 108
108 85 LVDS_L_DATA_P<3>	23	24	
85 GPU_DDC_C_CLK	25	26	GPU_DDC_C_DATA 85
	27	28	
	29	30	

90 =PP3V3_DDC_LCD
90 6 PPV_LCD_CONN
PPV_LCD_CONN 6 90

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9010 0.001uF 20% 50V CERM 402

CRITICAL
SDF9001
STDOFF-3MMOD4.6MMH-1.35-TH

INVERTER INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

85 GPU_VARY_BL
R9075 47 5% 1/16W MF-LF 402 — LCD_PWM 6
NOSTUFF
R9074 10K 5% 1/16W MF-LF 402

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INTERNAL DISPLAY CONNS

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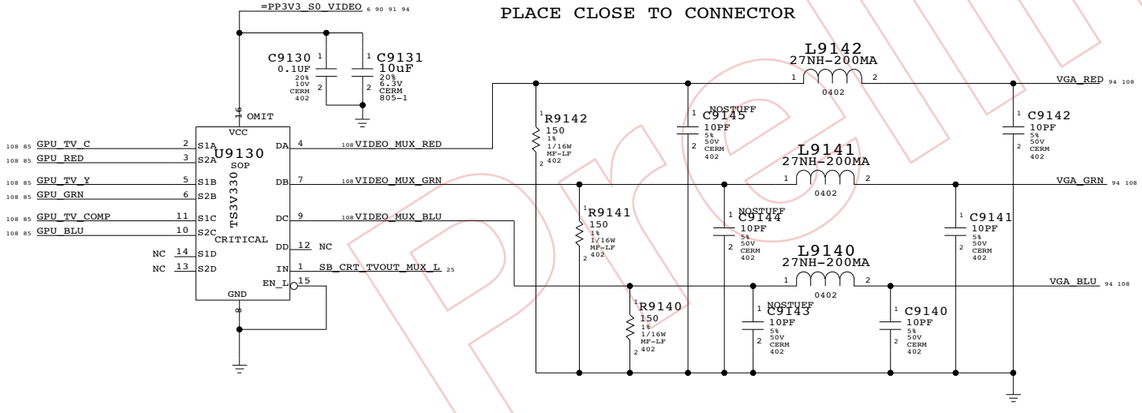
ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

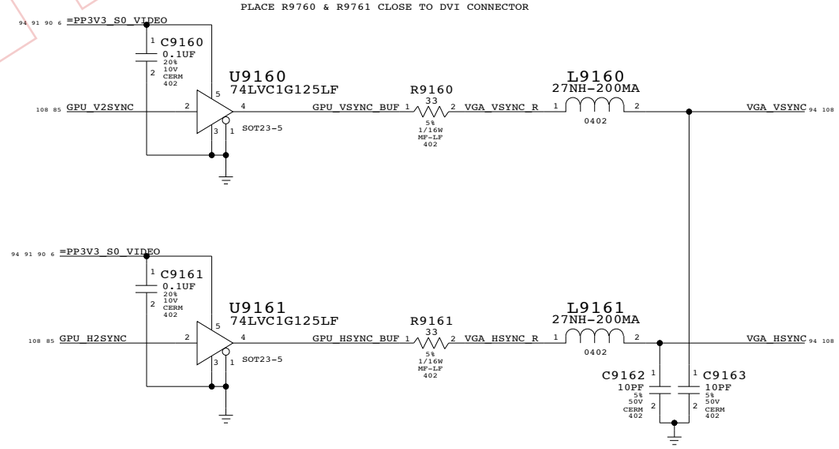


VIDEO_MUX_SEL	OUT
1	CRT
0	TV

PLACE U9120 NEAR GMCH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1700	1	QUAD SPDT HIGH-BANDWITDH VIDEO SWITCH,LOW ON-RES	U9130	CRITICAL	

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



Analog Video Support

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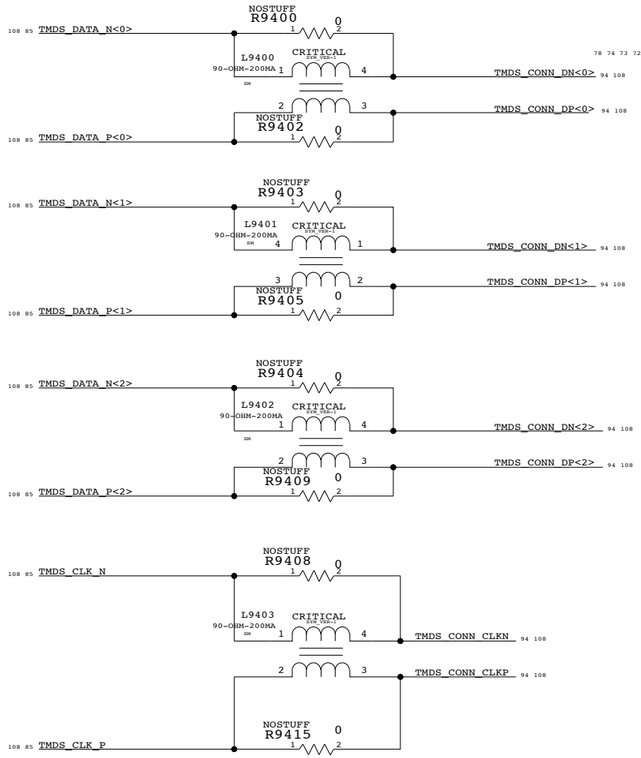
DVI INTERFACE

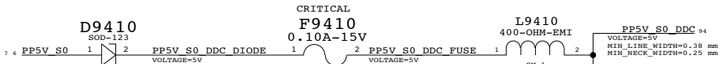
TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

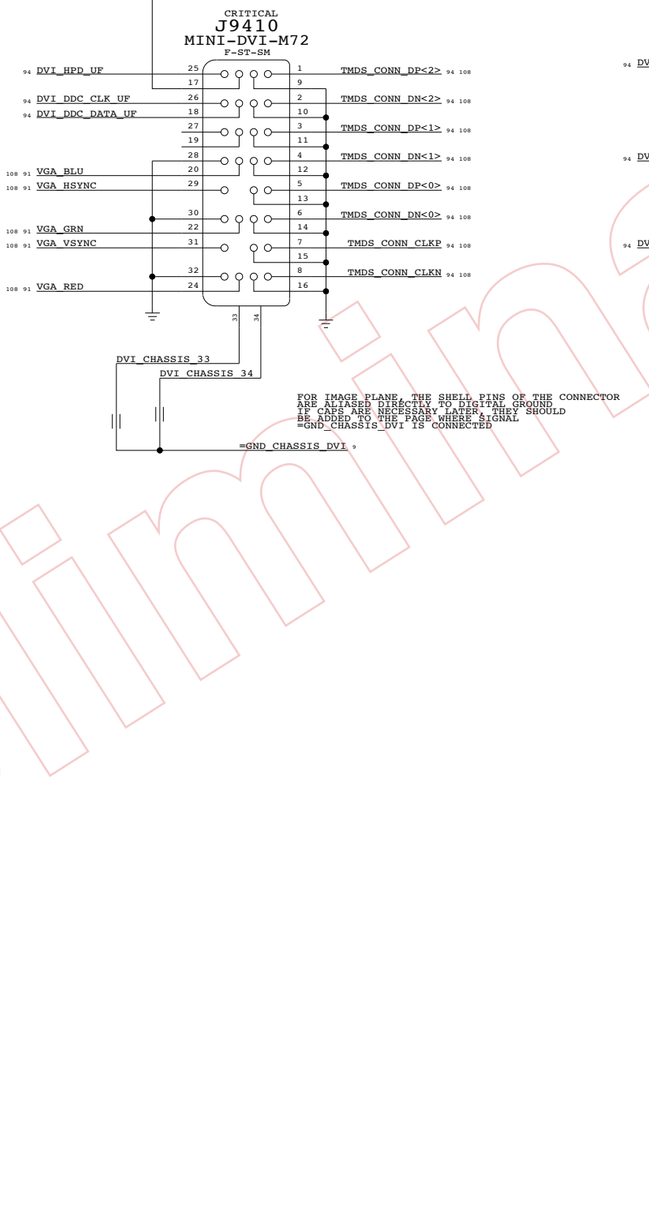


DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)



DON'T USE M51 SPECIFIC: 514S0129
APPLE PN: 514S0167



FOR IMAGE PLANE, THE SHELL PINS OF THE CONNECTOR ARE ALIASED DIRECTLY TO DIGITAL GROUND IF CAPS ARE NECESSARY LATER, THEY SHOULD BE ADDED TO THE PAGE WHERE SIGNAL =GND_CHASSIS_DVI IS CONNECTED

PLACE CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS

Note: this clamp is supposed to be on the MXM card

R9414 SHOULD BE GREATER THAN 0 IF MXM CARD DOES NOT HAVE A CURRENT LIMITING RESISTOR ON THIS LINE

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External Display Conns

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CRITICAL
SDF9800
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9801
STDOFF-4.0OD3.5H-1.35-TH

APN 518S0502

CRITICAL
J9800
52893-2095
F-RT-SM

9 GND_AUDIO_SPKRAMP
C9800 1UF 10V 25V X7R 805
6 =PP12V_S0_AUDIO_SPKRAMP
98 6 =PP5V_S0_AUDIO
103 23 HDA_SDIN0
103 23 HDA_SDOUT
103 23 HDA_BIT_CLK
103 23 HDA_RST_L
103 23 HDA_SYNC
98 6 =PP3V3_S0_AUDIO

=PP5V_S0_AUDIO 6 98
=PP3V3_S0_AUDIO 6 98
NOSTUFF C9801 0.1UF 20% 10V CERM 402
NOSTUFF C9802 0.1UF 20% 10V CERM 402

CRITICAL
SDF9803
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9804
STDOFF-4.0OD3.5H-1.35-TH

STANDOFFS ARE 860-0893

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MLB: AUDIO CONNECTOR

SYNC_MASTER=DEREK SYNC_DATE=1/26/2007

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	*	*	SPACING_0.2MM
FSB_ADSTB	*	*	SPACING_0.3MM
FSB_DATA	*	*	SPACING_0.2MM
FSB_DSTB	*	*	SPACING_0.3MM
FSB_COMMON	*	*	SPACING_0.2MM

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_55S	*	55_OHM_SE
CPU_27P4S	*	27P4_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_2TO1	*	*	SPACING_0.2MM
CPU_COMP	*	*	SPACING_0.6MM
CPU_GTLREF	*	*	SPACING_0.6MM
CPU_ITP	*	*	SPACING_0.2MM
CPU_VCCSENSE	*	*	SPACING_0.6MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON_2PP	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..1>	10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_D_L<0>	7 10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..17>	10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_D_L<16>	7 10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..42>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_D_L<41>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<40..32>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..60>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_D_L<59>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<58..48>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..7>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<5..3>	10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_A_L<6>	7 10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..28>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<26..17>	10 14
FSB_ADDR_GROUP1_PP	FSB_55S	FSB_ADDR	FSB_A_L<27>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 50
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB_PP	CPU_55S		CPU_INTR	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_NMI	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_A20M_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	10 23
CPU_FROM_SB_PP	CPU_55S		CPU_IGNNE_L	7 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	7 10 23 51
CPU_FROM_SB_PP	CPU_55S		CPU_SMI_L	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 50
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	16 25 71
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	71
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	10 16 23 71
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 105
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 105
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP_CPURST_L	
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71

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CPU/FSB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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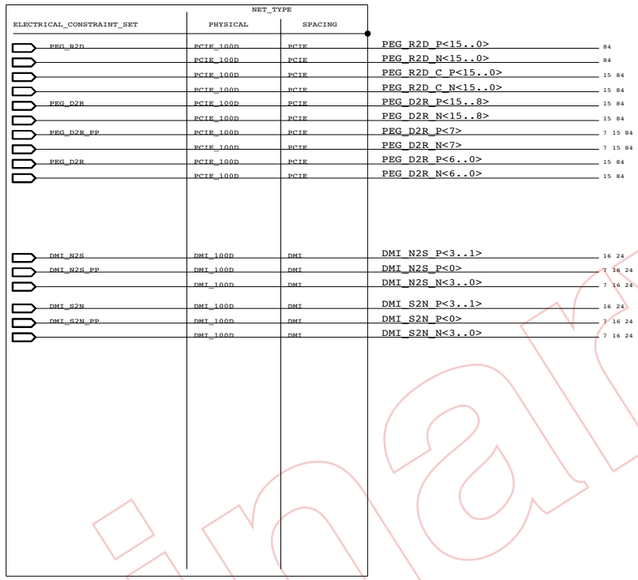
D	051-7228	27
SCALE: NONE	SHT 100 OF 118	

PCI-Express / DMI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_OHM_DIFF
DMI_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	SPACING_0.5MM
DMI	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5



Video Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	100_OHM_DIFF
CRT_55S	*	55_OHM_SE
CRT_50S	*	50_OHM_SE
TMDS_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
LVDS	*	*	SPACING_0.5MM	
CRT	*	*	SPACING_0.6MM	DG Says 40 mil spacing minimum
CRT	CRT	*	SPACING_0.5MM	
TVDAC				
				DG Says 30 mil spacing minimum
CRT_SYNC	*	*	SPACING_0.6MM	
CRT_SYNC	CRT_SYNC	*	SPACING_0.5MM	
TMDS	*	*	SPACING_0.5MM	DG Says 40 mil spacing minimum

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

Preliminary

NB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE	SHT	OF
NONE	101	118

DDR2 Memory Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_45S	*	45_OHM_SE
MEM_55S	*	55_OHM_SE
MEM_70D	*	70_OHM_DIFF
MEM_85D	*	85_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	SPACING_0.6MM
MEM_CMD	*	*	SPACING_0.15MM
MEM_CTRL	*	*	SPACING_0.6MM
MEM_DATA	*	*	SPACING_0.6MM
MEM_DQS	*	*	SPACING_0.6MM
MEM_CLK	MEM_CLK	*	SPACING_0.4MM
MEM_CLK	MEM_CTRL	*	SPACING_0.4MM
MEM_CLK	MEM_CMD	*	SPACING_0.4MM
MEM_CLK	MEM_DATA	*	SPACING_0.4MM
MEM_CLK	MEM_DQS	*	SPACING_0.4MM
MEM_CTRL	MEM_CTRL	*	SPACING_0.2MM
MEM_CTRL	MEM_CMD	*	SPACING_0.3MM
MEM_CTRL	MEM_DATA	*	SPACING_0.3MM
MEM_CTRL	MEM_DQS	*	SPACING_0.3MM
MEM_CMD	MEM_CMD	*	SPACING_0.15MM
MEM_CMD	MEM_DATA	*	SPACING_0.3MM
MEM_CMD	MEM_DQS	*	SPACING_0.3MM
MEM_DATA	MEM_DATA	*	SPACING_0.15MM
MEM_DATA	MEM_DQS	*	SPACING_0.3MM
MEM_DQS	MEM_DQS	*	SPACING_0.3MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<1..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<1..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<6..0>	17 31
MEM_A_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_A_DQ<7>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<13..8>	17 31
MEM_A_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_A_DQ<14>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15>	17 31
MEM_A_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_A_DQ<16>	7 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..17>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<24>	17 31
MEM_A_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_A_DQ<25>	7 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..26>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<38..32>	17 31
MEM_A_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_A_DQ<39>	7 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<46..40>	17 31
MEM_A_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_A_DQ<47>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<53..48>	17 31
MEM_A_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_A_DQ<54>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<58..56>	17 31
MEM_A_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_A_DQ<59>	7 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..60>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	7 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	7 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	7 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	7 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	7 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	7 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	7 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	7 17 31

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<4..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<4..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 31 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<5..0>	17 32
MEM_B_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_B_DQ<6>	7 17 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7>	17 32
MEM_B_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_B_DQ<8>	7 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..9>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<22..16>	17 32
MEM_B_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_B_DQ<23>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<24>	17 32
MEM_B_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_B_DQ<25>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..26>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<37..32>	17 32
MEM_B_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_B_DQ<38>	7 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<43..40>	17 32
MEM_B_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_B_DQ<44>	7 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..45>	17 32
MEM_B_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_B_DQ<48>	7 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..49>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<61..56>	17 32
MEM_B_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_B_DQ<62>	7 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	7 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	7 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	7 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	7 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	7 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	7 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	7 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	7 17 32

Preliminary

Memory Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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SIZE D | DRAWING NUMBER 051-7228 | REV. 27

SCALE NONE | SHT 102 OF 118

Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18MM

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..10> 23 44
IDE_PDD_EP	IDE_55S	IDE	IDE_PDD<9> 7 23 44
IDE_PDD	IDE_55S	IDE	IDE_PDD<8..0> 23 44
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 23 44
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 7 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 23 44
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 7 23 44
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 44
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L 24 44
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 23 45
	SATA_100D	SATA	SATA_A_R2D_C_N 23 45
	SATA_100D	SATA	SATA_A_R2D_P 45
	SATA_100D	SATA	SATA_A_R2D_N 45
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P 7 23 45
	SATA_100D	SATA	SATA_A_D2R_N 7 23 45
	SATA_100D	SATA	SATA_A_D2R_C_P 45
	SATA_100D	SATA	SATA_A_D2R_C_N 45
	SATA_100D	SATA	SATA_B_R2D_C_P 23 45
	SATA_100D	SATA	SATA_B_R2D_C_N 23 45
	SATA_100D	SATA	SATA_B_D2R_P 23 45
	SATA_100D	SATA	SATA_B_D2R_N 23 45
SATA_RBIAS	SATA_55S		SATA_RBIAS 45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 98
	HDA_55S	HDA	HDA_BIT_CLK_R 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 98
	HDA_55S	HDA	HDA_SYNC_R 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 23 98
	HDA_55S	HDA	HDA_RST_L_R 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 98
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 98
	HDA_55S	HDA	HDA_SDOUT_R 23
USB_EXTA	USB_90D	USB	USB_EXTA_P 24 46
	USB_90D	USB	USB_EXTA_N 24 46
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 24 34
	USB_90D	USB	USB_MINI_N 24 34
	USB_90D	USB	USB_EXTD_P 24 46
	USB_90D	USB	USB_EXTD_N 24 46
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 7 24 47
	USB_90D	USB	USB_CAMERA_N 7 24 47
USB_BT	USB_90D	USB	USB_BT_P 7 24 47
	USB_90D	USB	USB_BT_N 7 24 47
	USB_90D	USB	USB_TPAD_P 24 47
	USB_90D	USB	USB_TPAD_N 24 47
USB_IR	USB_90D	USB	USB_IR_P 7 24 47
	USB_90D	USB	USB_IR_N 7 24 47
USB_EXTB	USB_90D	USB	USB_EXTB_P 24 46
	USB_90D	USB	USB_EXTB_N 24 46
	USB_90D	USB	USB_EXCARD_P 24 47
	USB_90D	USB	USB_EXCARD_N 24 47
USB_EXTC	USB_90D	USB	USB_EXTC_P 24 46
	USB_90D	USB	USB_EXTC_N 24 46
USB_RBIAS	USB_60S		USB_RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK 25 52
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA 25 52
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK 25 52
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA 25 52
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 24 61
	SPI_55S	SPI	SPI_SCLK 7 61
	SPI_55S	SPI	SPI_A_SCLK_R
	SPI_55S	SPI	SPI_B_SCLK_R
SPI_SI	SPI_55S	SPI	SPI_SI_R 24 61
	SPI_55S	SPI	SPI_SI
	SPI_55S	SPI	SPI_A_SI_R 61
	SPI_55S	SPI	SPI_B_SI_R
SPI_SO	SPI_55S	SPI	SPI_SO 7 24 61
	SPI_55S	SPI	SPI_A_SO_R 7 61
	SPI_55S	SPI	SPI_B_SO
	SPI_55S	SPI	SPI_B_SO_R
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 24 61
	SPI_55S	SPI	SPI_CE_L<0> 7 61
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>
	SPI_55S	SPI	SPI_CE_L<1>

Preliminary

SB Constraints (1 of 2)

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7228	27
SCALE: NONE	SHT 103 OF 118	

PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_AD<18..0>	24 28
	PCI_55S	PCI	PCI_AD<19>	24 28
	PCI_55S	PCI	PCI_AD<20>	24 28
	PCI_55S	PCI	PCI_AD<31..21>	24 28
	PCI_55S	PCI	PCI_PAR	24 28
	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 28
	PCI_55S	PCI	PCI_IRDY_L	24
	PCI_55S	PCI	PCI_DEVSEL_L	24
	PCI_55S	PCI	PCI_PERR_L	24
	PCI_55S	PCI	PCI_LOCK_L	24
	PCI_55S	PCI	PCI_SERR_L	24 28
	PCI_55S	PCI	PCI_STOP_L	24
	PCI_55S	PCI	PCI_TRDY_L	24
	PCI_55S	PCI	PCI_FRAME_L	24
	PCI_55S	PCI	PCI_FW_REQ_L	24
	PCI_55S	PCI	PCI_FW_GNT_L	24
	PCI_55S	PCI	PCI_REQ1_L	7 24
	PCI_55S	PCI	PCI_GNT1_L	
	PCI_55S	PCI	PCI_REQ2_L	7 24
	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	7 24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	7 24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 37
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	7 24 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	7 24 37
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	40 42
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	40 42
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	7 40 42
	PCIE_100D	PCIE	PCIE_FW_D2R_N	7 40 42
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	7 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	7 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
E14		PWR	PP1V9R2V5_ENET_PHY_AVDD	37 39
E15		PWR	PP1V9R2V5_S3_ENET_R	38
E13		ENET_MDI_TERM	ENET_MDI0	37
E12		ENET_MDI_TERM	ENET_MDI1	37
E11		ENET_MDI_TERM	ENET_MDI2	37
E10		ENET_MDI_TERM	ENET_MDI3	37
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	37 39
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	37 39
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	37 39
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	37 39

Preliminary

SB Constraints (2 of 2)

SYNC_MASTER=(MASTER) SYNC_DATE=(10/02/2006)

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE: NONE

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_FSB_100D	*	100_OHM_DIFF
CLK_PCIE_100D	*	100_OHM_DIFF
CLK_MED_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	*	*	CLK_SPACING_0.6MM
CLK_PCIE	*	*	CLK_SPACING_0.5MM
CLK_MED	*	*	CLK_SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 100
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 100
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 51
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	7 24 30
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	7 30 49
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	7 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	7 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	30 85
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	30 85
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	7 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	7 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7 30 40
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7 30 40
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	7 23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	7 23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 30 37
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 30 37

Preliminary

Clock Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7228	27

SCALE: NONE SHT 105 OF 118

FireWire Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FW_110D	*	110_OHM_DIFF
FW_110D	BGA_P1MM	110_OHM_DIFF_ESCAPE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FW_TP	*	*	SPACING_0.3MM

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	43
	FW_110D	FW_TP	FW_PORT0_TPA_N	43
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	43
	FW_110D	FW_TP	FW_PORT0_TPB_N	43
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_N	43
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_N	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_N	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_N	43

Port 2 Not Used

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	52
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	52
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	52
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	52
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	52
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	52
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	52
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	52

Preliminary

FireWire & SMC Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	900
PWR	*	=STANDARD	900

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PWR	*	PWR_P2MM
MEM_CMD	PWR	*	PWR_P2MM
MEM_CTRL	PWR	*	PWR_P2MM
MEM_DATA	PWR	*	PWR_P2MM
MEM_DQS	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	PWR	*	PWR_P2MM
DMI	PWR	*	PWR_P2MM
SATA	PWR	*	PWR_P2MM
USB	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	PWR	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	SPACING_0.4MM
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
SMS	*	*	SPACING_0.3MM

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<3..0> 85 94
	TMDS_100D	TMDS	TMDS_DATA_N<3..0> 85 94
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P 85 94
	TMDS_100D	TMDS	TMDS_CLK_N 85 94
	TMDS_100D	TMDS	TMDS_CONN_DP<3..0> 94
	TMDS_100D	TMDS	TMDS_CONN_DN<3..0> 94
	TMDS_100D	TMDS	TMDS_CONN_CLKP 94
	TMDS_100D	TMDS	TMDS_CONN_CLKN 94
(USB_EXTA)	USB_90D	USB	USB_PORT0_P 46
(USB_EXTA)	USB_90D	USB	USB_PORT0_N 46
(USB_EXTB)	USB_90D	USB	USB_PORT1_P 46
(USB_EXTB)	USB_90D	USB	USB_PORT1_N 46
(USB_EXTC)	USB_90D	USB	USB_PORT2_P 46
(USB_EXTC)	USB_90D	USB	USB_PORT2_N 46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_P 46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_N 46
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_P 47
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_N 47
(USB_IR)	USB_90D	USB	USB_IR_L_P 47 58
(USB_IR)	USB_90D	USB	USB_IR_L_N 47 58
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P 85 90
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_N 85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0> 85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0> 85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P 85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_N 85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0> 85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0> 85 90
	PCIE_100D	PCIE	PCIE_FW_R2D_N 7 40
	PCIE_100D	PCIE	PCIE_FW_R2D_P 7 40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_N 40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_P 40
	PCIE_100D	PCIE	PCIE_ENET_R2D_P 7 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_N 7 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N 37
	PCIE_100D	PCIE	PCIE_MINI_R2D_N 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_P 34
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<0> 39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<0> 39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<1> 39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<1> 39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<2> 39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<2> 39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<3> 39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<3> 39
	ENET_100D	ENET_MDI	ENET_MDI_R_P<0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<0>
	ENET_100D	ENET_MDI	ENET_MDI_R_P<1>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<1>
	ENET_100D	ENET_MDI	ENET_MDI_R_P<2>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<2>
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3>
	CRT_50S	CRT	GPU_TV_COMP 85 91
	CRT_50S	CRT	GPU_TV_C 85 91
	CRT_50S	CRT	GPU_TV_Y 85 91
CRT_RED	CRT_50S	CRT	GPU_RED 85 91
CRT_GREEN	CRT_50S	CRT	GPU_GRN 85 91
CRT_BLUE	CRT_50S	CRT	GPU_BLU 85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_H2SYNC 85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_V2SYNC 85 91
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_HSYNC 91 94
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_VSYNC 91 94
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_HSYNC
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_VSYNC
	CRT_50S	CRT	VIDEO_MUX_RED 91
	CRT_50S	CRT	VIDEO_MUX_GRN 91
	CRT_50S	CRT	VIDEO_MUX_BLU 91
	CRT_55S	CRT	VGA_RED 91 94
	CRT_55S	CRT	VGA_GRN 91 94
	CRT_55S	CRT	VGA_BLU 91 94
THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_P 55
	THERM_DIFF	THERMAL	HDD_THRMD_N 55
THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_P 55
	THERM_DIFF	THERMAL	ODD_THRMD_N 55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P 10 55
	THERM_DIFF	THERMAL	CPU_THERMD_N 10 55
THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_P 55
	THERM_DIFF	THERMAL	GPU_HSK_THRMD_N 55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_P 55
	THERM_DIFF	THERMAL	CPU_HSK_THRMD_N 55

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
E156		SWITCHNODE	IMVP6_PHASE1 71
E155		SWITCHNODE	IMVP6_PHASE2 71
E157		SWITCHNODE	IMVP6_PHASE3 72
E158		SWITCHNODE	1V05REG_SWITCHNODE 73
E159		SWITCHNODE	1V5REG_SWITCHNODE 73
E160		SWITCHNODE	MCH_CORES0_SWITCHNODE 74
E161		SWITCHNODE	1V25REG_SWITCHNODE 74
E154		SWITCHNODE	1V8S3_PHASE 75
E162		SWITCHNODE	5VS5_SW 76
E163		SWITCHNODE	3V3S3_SW 76
E164		SWITCHNODE	P3V3S5_SW 77
E165		SWITCHNODE	P2V5S0_SW 77
E166		SMS	SMS_X_AXIS 49 50
E167		SMS	SMS_Y_AXIS 49 50
E168		SMS	SMS_Z_AXIS 49 50

M72/M78 SPECIFIC CONSTRAINTS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
DEFAULT	TOP,BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
55_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
40_OHM_SE	*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
45_OHM_SE	*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.340 MM	0.340 MM			
27P4_OHM_SE	*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF_ESCAPE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF_ESCAPE	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.250 MM	0.250 MM
110_OHM_DIFF_ESCAPE	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.15 MM	0.15 MM			
50_OHM_SE	*	Y	0.120 MM	0.120 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_MED	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPACING_0.15MM	*	0.15 MM	?
SPACING_0.18MM	*	0.18 MM	?
SPACING_0.2MM	*	0.2 MM	?
SPACING_0.25MM	*	0.25 MM	?
SPACING_0.3MM	*	0.3 MM	?
SPACING_0.4MM	*	0.4 MM	?
SPACING_0.5MM	*	0.5 MM	?
SPACING_0.6MM	*	0.6 MM	?
SWITCHNODE	*	0.6 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
CLK_SPACING_0.5MM	TOP,BOTTOM	0.2 MM	?
CLK_SPACING_0.6MM	TOP,BOTTOM	0.2 MM	?

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M72/M78 RULE DEFINITIONS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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D	051-7228	27
SCALE: NONE	SHT 109 OF 118	

Title: Basenet Report
Design: m72
Date: Mar 23 10:23:45 2007

Base nets and synonyms for m72_lib.M72(@m72_lib.m72(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V9S0_COMP_REF	0V9S0_COMP_REF - @m72_lib.M72	70C6
1V05REG_BOOT	1V05REG_BOOT - @m72_lib.M72	73C4
1V05REG_BOOT_R	1V05REG_BOOT_R - @m72_lib.M72	73C3
1V05REG_ISEN	1V05REG_ISEN - @m72_lib.M72	73C4
1V05REG_LGATE	1V05REG_LGATE - @m72_lib.M72	73C3
1V05REG_OCSET	1V05REG_OCSET - @m72_lib.M72	73B4
1V05REG_SNUBBER_R	1V05REG_SNUBBER_R - @m72_lib.M72	73C2
1V05REG_SOFT	1V05REG_SOFT - @m72_lib.M72	73C4
1V05REG_SWITCHNODE	1V05REG_SWITCHNODE - @m72_lib.M72	73B3 108D1
1V05REG_UGATE	1V05REG_UGATE - @m72_lib.M72	73C4
1V05REG_VSEN	1V05REG_VSEN - @m72_lib.M72	73B3
1V05S0_EN	1V05S0_EN - @m72_lib.M72	73B4
1V05S0_RUNSS	1V05S0_RUNSS - @m72_lib.M72	70C5 73C3 74C3
1V05S0_RUNSS_BUF	1V05S0_RUNSS_BUF - @m72_lib.M72	70C6
1V5REG_BOOT	1V5REG_BOOT - @m72_lib.M72	73C5
1V5REG_BOOT_R	1V5REG_BOOT_R - @m72_lib.M72	73C6
1V5REG_ISEN	1V5REG_ISEN - @m72_lib.M72	73C5
1V5REG_LGATE	1V5REG_LGATE - @m72_lib.M72	73C5
1V5REG_OCSET	1V5REG_OCSET - @m72_lib.M72	73B5
1V5REG_SNUBBER_R	1V5REG_SNUBBER_R - @m72_lib.M72	73B7
1V5REG_SOFT	1V5REG_SOFT - @m72_lib.M72	73C5
1V5REG_SWITCHNODE	1V5REG_SWITCHNODE - @m72_lib.M72	73C6 108D1
1V5REG_UGATE	1V5REG_UGATE - @m72_lib.M72	73C5
1V5REG_VSEN	1V5REG_VSEN - @m72_lib.M72	73B7
1V5S0_RUNSS	1V5S0_RUNSS - @m72_lib.M72	70A5 73C5
1V5S0_RUNSS_BUF	1V5S0_RUNSS_BUF - @m72_lib.M72	70A6
1V8S0_COMP_REF	1V8S0_COMP_REF - @m72_lib.M72	70D6
1V8S3_BOOT	1V8S3_BOOT - @m72_lib.M72	75C5
1V8S3_BOOT_RC	1V8S3_BOOT_RC - @m72_lib.M72	75D5
1V8S3_COMP	1V8S3_COMP - @m72_lib.M72	75C6
1V8S3_COMP_R	1V8S3_COMP_R - @m72_lib.M72	75C6
1V8S3_EN	1V8S3_EN - @m72_lib.M72	75C6
1V8S3_FB	1V8S3_FB - @m72_lib.M72	75C6
1V8S3_FCCM	1V8S3_FCCM - @m72_lib.M72	75C6
1V8S3_FSET	1V8S3_FSET - @m72_lib.M72	75C6
1V8S3_ISEN	1V8S3_ISEN - @m72_lib.M72	75C5
1V8S3_LG	1V8S3_LG - @m72_lib.M72	75C5
1V8S3_PHASE	1V8S3_PHASE - @m72_lib.M72	75C5 108D1
1V8S3_SNUBBER_R	1V8S3_SNUBBER_R - @m72_lib.M72	75C3
1V8S3_UG	1V8S3_UG - @m72_lib.M72	75C5
1V8S3_VCC	1V8S3_VCC - @m72_lib.M72	75D6
1V25REG_BOOT	1V25REG_BOOT - @m72_lib.M72	74C5
1V25REG_BOOT_R	1V25REG_BOOT_R - @m72_lib.M72	74C6
1V25REG_ISEN	1V25REG_ISEN - @m72_lib.M72	74C5
1V25REG_LGATE	1V25REG_LGATE - @m72_lib.M72	74C5
1V25REG_OCSET	1V25REG_OCSET - @m72_lib.M72	74B5
1V25REG_SNUBBER_R	1V25REG_SNUBBER_R - @m72_lib.M72	74B7
1V25REG_SOFT	1V25REG_SOFT - @m72_lib.M72	74C5
1V25REG_SWITCHNODE	1V25REG_SWITCHNODE - @m72_lib.M72	74C6 108D1
1V25REG_UGATE	1V25REG_UGATE - @m72_lib.M72	74C5
1V25REG_VSEN	1V25REG_VSEN - @m72_lib.M72	74B7
1V25S0_RUNSS	1V25S0_RUNSS - @m72_lib.M72	70B5 74C5
1V25S0_RUNSS_BUF	1V25S0_RUNSS_BUF - @m72_lib.M72	70B6
3V3S0_COMP_REF	3V3S0_COMP_REF - @m72_lib.M72	70D6
3V3S3_BG	3V3S3_BG - @m72_lib.M72	76B5
3V3S3_BOOST	3V3S3_BOOST - @m72_lib.M72	76B5
3V3S3_BOOST_R	3V3S3_BOOST_R - @m72_lib.M72	76C6
3V3S3_ITH	3V3S3_ITH - @m72_lib.M72	76B5
3V3S3_ITH_R	3V3S3_ITH_R - @m72_lib.M72	76B6
3V3S3_RUNSS	3V3S3_RUNSS - @m72_lib.M72	76B5
3V3S3_SNS_N	3V3S3_SNS_N - @m72_lib.M72	76C6
3V3S3_SNS_P	3V3S3_SNS_P - @m72_lib.M72	76C6
3V3S3_SW	3V3S3_SW - @m72_lib.M72	76B5 108D1
3V3S3_TG	3V3S3_TG - @m72_lib.M72	76C5
3V3S3_VOSNS	3V3S3_VOSNS - @m72_lib.M72	76B5
5VS0_COMP_REF	5VS0_COMP_REF - @m72_lib.M72	70C6
5VS3_COMP_REF	5VS3_COMP_REF - @m72_lib.M72	76A7
5VS5_0V76_REF	5VS5_0V76_REF - @m72_lib.M72	70C6
5VS5_1V53_REF	5VS5_1V53_REF - @m72_lib.M72	70D6
5VS5_2V80_REF	5VS5_2V80_REF - @m72_lib.M72	70D6
5VS5_4V24_REF1	5VS5_4V24_REF1 - @m72_lib.M72	70D6
5VS5_4V24_REF2	5VS5_4V24_REF2 - @m72_lib.M72	76A7
5VS5_4V29_REF	5VS5_4V29_REF - @m72_lib.M72	76D7
5VS5_BG	5VS5_BG - @m72_lib.M72	76B4
5VS5_BOOST	5VS5_BOOST - @m72_lib.M72	76B4
5VS5_BOOST_R	5VS5_BOOST_R - @m72_lib.M72	76C3
5VS5_ITH	5VS5_ITH - @m72_lib.M72	76B4
5VS5_ITH_R	5VS5_ITH_R - @m72_lib.M72	76B3
5VS5_RUNSS	5VS5_RUNSS - @m72_lib.M72	76B4
5VS5_SNS_N	5VS5_SNS_N - @m72_lib.M72	76C3
5VS5_SNS_P	5VS5_SNS_P - @m72_lib.M72	76C3
5VS5_SW	5VS5_SW - @m72_lib.M72	76B4 108D1
5VS5_TG	5VS5_TG - @m72_lib.M72	76C4
5VS5_VOSNS	5VS5_VOSNS - @m72_lib.M72	76B4
12VS0_6V0_REF	12VS0_6V0_REF - @m72_lib.M72	76D7
12VS0_COMP_REF	12VS0_COMP_REF - @m72_lib.M72	76D7
=ENET_CLKREQ_L	=ENET_CLKREQ_L - @m72_lib.M72	37B8 38D1
	ENET_CLKREQ_R_L - @m72_lib.M72	38D1
=ENET_VMAIN_AVLBL	=ENET_VMAIN_AVLBL - @m72_lib.M72	37C2 38A3
	PP3V3_S0 - @m72_lib.M72	6B8 6C6 6D7 7D3 13D6 70C3 70D3 70D8 77C6 78C3
	=PP3V3_DDC_LCD - @m72_lib.M72	90A8 90D5
	=PP3V3_S0_VIDEO - @m72_lib.M72	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_NB_VCCA_PEG_BG - @m72_lib.M72	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @m72_lib.M72	6A4 21C2
	=PP3V3_S0_TSENS - @m72_lib.M72	6A4 55B5 55D6 55D8
	=PP3V3_S0_SMC - @m72_lib.M72	6A4 53C2
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @m72_lib.M72	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @m72_lib.M72	6A4 26A3 27D4
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @m72_lib.M72	6B4 26C3
	=PP3V3R1V5_S0_SB_VCCHDA - @m72_lib.M72	6B4 26B3 27B4
	=PP3V3_S0_SB_VCC3_3_DMI - @m72_lib.M72	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_SATA - @m72_lib.M72	6B4 26C3 27C4
	=PP3V3_S0MWOL_SB_CLINK0 - @m72_lib.M72	6B4 25C1
	=PP3V3_S0M_CK505 - @m72_lib.M72	6B4 29D2 29D8 30D1
	=PP3V3_S0_SATALED - @m72_lib.M72	6B4 45C2
	=PP3V3_S0_MXM - @m72_lib.M72	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_CK505 - @m72_lib.M72	6B4 29C7 30D7
	=PP3V3_S0_SMBUS_SMC_B_S0 - @m72_lib.M72	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_MGMT - @m72_lib.M72	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_0_S0 - @m72_lib.M72	6B4 52D5
	=PP3V3_S0_SMC_LS - @m72_lib.M72	6B4 50D2
	=PP3V3_S0_LPCPLUS - @m72_lib.M72	6B4 51C4
	=PP3V3_S0_SMBUS_SB - @m72_lib.M72	6B4 52D8
	=PP3V3_S0_IMVP - @m72_lib.M72	6B4 71D8
	=PP3V3_S0_AUDIO - @m72_lib.M72	6B4 98C4 98C6
	=PPSPD_S0_MEM - @m72_lib.M72	6B4 31A7 32A3 32A7
	=PP3V3_S0_FAN - @m72_lib.M72	6B4 56B7 56C7 57C7
	=PP3V3_S0_SB_PM - @m72_lib.M72	6B4 28A7
	=PP3V3_S0_PATA - @m72_lib.M72	6B4 44C6
	=PP3V3_S0_SB_PCI - @m72_lib.M72	6B4 24A3
	=PP3V3_S0_SB_VCC3_3_IDE - @m72_lib.M72	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_PCI - @m72_lib.M72	6B4 26B3 27C4
	=PP3V3_S0_SB_GPIO - @m72_lib.M72	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @m72_lib.M72	6B4 26A6
	=PP3V3_S0_SB - @m72_lib.M72	6C4 27D8
	=PP3V3_S0_NB_VCCHV - @m72_lib.M72	6C4 16B7 16C7 16C7 19B3 21A8
	PP3V3_S0 - @m72_lib.M72	6B8 6C6 6D7 7D3 13D6 70C3 70D3 70D8 77C6 78C3
	=PPSPD_S0_MEM - @m72_lib.M72	6B4 31A7 32A3 32A7
	=PP3V3_S0_VIDEO - @m72_lib.M72	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_TSENS - @m72_lib.M72	6A4 55B5 55D6 55D8
	=PP3V3_S0_SMC_LS - @m72_lib.M72	6B4 50D2
	=PP3V3_S0_SMC - @m72_lib.M72	6A4 53C2
	=PP3V3_S0_SMBUS_SMC_MGMT - @m72_lib.M72	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_B_S0 - @m72_lib.M72	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_0_S0 - @m72_lib.M72	6B4 52D5
	=PP3V3_S0_SMBUS_SB - @m72_lib.M72	6B4 52D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @m72_lib.M72	6B4 26A6
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @m72_lib.M72	6B4 26C3
	=PP3V3_S0_SB_VCC3_3_SATA - @m72_lib.M72	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_PCI - @m72_lib.M72	6B4 26B3 27C4
	=PP3V3_S0_SB_VCC3_3_IDE - @m72_lib.M72	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_DMI - @m72_lib.M72	6B4 26C3 27C4
	=PP3V3_S0_SB_PM - @m72_lib.M72	6B4 28A7
	=PP3V3_S0_SB_PCI - @m72_lib.M72	6B4 24A3
	=PP3V3_S0_SB_GPIO - @m72_lib.M72	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB - @m72_lib.M72	6C4 27D8
	=PP3V3_S0_SATALED - @m72_lib.M72	6B4 45C2
	=PP3V3_S0_PATA - @m72_lib.M72	6B4 44C6
	=PP3V3_S0_NB_VCCHV - @m72_lib.M72	6C4 16B7 16C7 16C7 19B3 21A8
	=PP3V3_S0_NB_VCCA_PEG_BG - @m72_lib.M72	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @m72_lib.M72	6A4 21C2
	=PP3V3_S0_MXM - @m72_lib.M72	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_LPCPLUS - @m72_lib.M72	6B4 51C4
	=PP3V3_S0_IMVP - @m72_lib.M72	6B4 71D8
	=PP3V3_S0_FAN - @m72_lib.M72	6B4 56B7 56C7 57C7
	=PP3V3_S0_ENET - @m72_lib.M72	6A4 38A1
	=PP3V3_S0_CK505 - @m72_lib.M72	6B4 29C7 30D7
	=PP3V3_S0_AUDIO - @m72_lib.M72	6B4 98C4 98C6
	=PP3V3_S0M_CK505 - @m72_lib.M72	6B4 29D2 29D8 30D1
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @m72_lib.M72	6A4 26A3 27D4
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @m72_lib.M72	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_CLINK0 - @m72_lib.M72	6B4 25C1
	=PP3V3R1V5_S0_SB_VCCHDA - @m72_lib.M72	6B4 26B3 27B4
=GFX_VR_EN	=GFX_VR_EN - @m72_lib.M72	16B3 22A8
	TP_GFX_VR_EN - @m72_lib.M72	22A7
=GND_NB_VSSA_LVDS	=GND_NB_VSSA_LVDS - @m72_lib.M72	19C6 22C1
	TP_NB_VSSA_LVDS - @m72_lib.M72	22C2
=NB_CLINK_MPWROK	=NB_CLINK_MPWROK - @m72_lib.M72	16A3 22C2
	VR_PWRGOOD_DELAY - @m72_lib.M72	7C4 7C7 16B6 22C1 70C2 71C7
=PP0V9_S0M_MEM_TERM	=PP0V9_S0M_MEM_TERM - @m72_lib.M72	6D4 33D5
	PP0V9_S0 - @m72_lib.M72	6D6 7D3 70C8 75A3
=PP0V9_S3M_MEM_NBVREFA	=PP0V9_S3M_MEM_NBVREFA - @m72_lib.M72	7C7 16C2 22B1
	PP0V9_S3M_MEM_NBVREFA - @m72_lib.M72	22B2
=PP0V9_S3M_MEM_NBVREFB	=PP0V9_S3M_MEM_NBVREFB - @m72_lib.M72	7C7 16C2 22A1
	PP0V9_S3M_MEM_NBVREFB - @m72_lib.M72	22A2
=PP0V9_S3_MEM_A_VREF	=PP0V9_S3_MEM_A_VREF - @m72_lib.M72	31C1 31D6
	PP0V9_S3_MEM_A_VREF - @m72_lib.M72	31C2
=PP0V9_S3_MEM_B_VREF	=PP0V9_S3_MEM_B_VREF - @m72_lib.M72	32C1 32D7
	PP0V9_S3_MEM_B_VREF - @m72_lib.M72	32C2
=PP1V2_ENET_PHY	=PP1V2_ENET_PHY - @m72_lib.M72	37D6 38A3
	PP1V2_S3_ENET - @m72_lib.M72	38A3
=PP1V05_S0M_NB_VCCAXM	=PP1V05_S0M_NB_VCCAXM - @m72_lib.M72	6C4 18B3 18C1 21D8
	=PP1V05_S0_NB_FOLLOW - @m72_lib.M72	6C4 21C4
	=PPVCORE_S0_SB - @m72_lib.M72	6C4 26D3 27B1
	PP1V05_S0 - @m72_lib.M72	6C6 7D3 34C3 73A4 73C1
	=PP1V05_S0_NB_PCIE - @m72_lib.M72	6C4 21D5
	PP1V05_S0 - @m72_lib.M72	6C6 7D3 34C3 73A4 73C1
	=PPVCORE_S0_SB - @m72_lib.M72	6C4 26D3 27B1
	=PP1V05_S0_NB_PCIE - @m72_lib.M72	6C4 21D5
	=PP1V05_S0_NB_FOLLOW - @m72_lib.M72	6C4 21C4
=PP1V05_S0_CPU	=PP1V05_S0_CPU - @m72_lib.M72	6D4 10B5 10B6 10C5 10D5 11C6 12A3 13D6 50D2
	=PP1V05_S0_SB_CPU_IO - @m72_lib.M72	6C4 23D2 26C3 27B2
	=PPVCORE_S0_NB_FOLLOW - @m72_lib.M72	6D4 21B4
	PPMCH_CORE_S0 - @m72_lib.M72	6D6 7D3 55A6 73A2 74C1
	=PP1V25R1V05_S0_NB_VTT - @m72_lib.M72	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @m72_lib.M72	6D4 14B7 30B8 30C8 30C8
	=PPVCORE_S0_NB - @m72_lib.M72	6D4 18D3 18D7 21D8
	PPMCH_CORE_S0 - @m72_lib.M72	6D6 7D3 55A6 73A2 74C1
	=PPVCORE_S0_NB_FOLLOW - @m72_lib.M72	6D4 21B4
	=PPVCORE_S0_NB - @m72_lib.M72	6D4 18D3 18D7 21D8
	=PP1V25R1V05_S0_NB_VTT - @m72_lib.M72	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @m72_lib.M72	6D4 14B7 30B8 30C8 30C8
	=PP1V05_S0_SB_CPU_IO - @m72_lib.M72	6C4 23D2 26C3 27B2
=PP1V5_S0_CPU	=PP1V5_S0_CPU - @m72_lib.M72	6C4 11B6 12B3
	=PP1V5_S0_MINI - @m72_lib.M72	6C4 34C2
	PP1V5_S0 - @m72_lib.M72	6C6 7D3 73C8
	=PP1V5_S0_SB - @m72_lib.M72	6C4 27C8
	PP1V5_S0_SB_VCCGLANPLL - @m72_lib.M72	26A6 27B6
	=PP1V5_S0_SB_VCC1_5_A - @m72_lib.M72	6C4 26B6
	=PP1V5_S0_SB_VCCUSBPLL - @m72_lib.M72	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m72_lib.M72	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m72_lib.M72	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m72_lib.M72	6C4 26B6 27D2
	=PP1V5_S0_NB_TVDAC - @m72_lib.M72	6C4 22B3
	PP1V5_S0 - @m72_lib.M72	6C6 7D3 73C8
	=PP1V5_S0_SB_VCCUSBPLL - @m72_lib.M72	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m72_lib.M72	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m72_lib.M72	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m72_lib.M72	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A - @m72_lib.M72	6C4 26B6
	=PP1V5_S0_SB - @m72_lib.M72	6C4 27C8
	=PP1V5_S0_NB_TVDAC - @m72_lib.M72	6C4 22B3
	=PP1V5_S0_MINI - @m72_lib.M72	6C4 34C2
=PP1V5_S0_SB_VCCGLAN1_5	=PP1V5_S0_SB_VCCGLAN1_5 - @m72_lib.M72	26A6 27B6
	PP1V5_S0_SB_VCC1_5_B - @m72_lib.M72	23D7 24C2 26D6 27C6
=PP1V8_S0_MXM	=PP1V8_S0_MXM - @m72_lib.M72	6D4 84C7
	PP1V8_S0 - @m72_lib.M72	6D6 7D3 70D8 78A5
=PP1V8_S3M_MEM_NB	=PP1V8_S3M_MEM_NB - @m72_lib.M72	6D3 16D2 18D7 21C8 22B3
	=PP1V8_S3M_NB_VCC - @m72_lib.M72	6D3 21A4
	=PP1V8_S3_ENET - @m72_lib.M72	6D3 38B8
	PP1V8_S3 - @m72_lib.M72	6D4 7D3 75C1 78B6
	=PP1V8_S3_MEMVTT - @m72_lib.M72	6D3 75B6
	=PP1V8_S3_MEM - @m72_lib.M72	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	PP1V8_S3 - @m72_lib.M72	6D4 7D3 75C1 78B6
	=PP1V8_S3_MEMVTT - @m72_lib.M72	6D3 75B6
	=PP1V8_S3_MEM - @m72_lib.M72	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	=PP1V8_S3_ENET - @m72_lib.M72	6D3 38B8
	=PP1V8_S3M_NB_VCC - @m72_lib.M72	6D3 21A4
=PP1V9R2V5_ENET_PHY	=PP1V9R2V5_ENET_PHY - @m72_lib.M72	37D7 38C1
	PP1V9R2V5_S3_ENET - @m72_lib.M72	38C3 38C4
=PP1V25_S0M_NB_PLL	=PP1V25_S0M_NB_PLL - @m72_lib.M72	6C4 21D3
	=PP1V25_S0M_NB_VCCD_HPLL - @m72_lib.M72	19A6 21D1
	=PP1V25_S0_SB_DMI - @m72_lib.M72	6C4 26C3 27C1
	PP1V25_S0 - @m72_lib.M72	6C6 7D3 74C8
	=PP1V25_S0_NB_VCC - @m72_lib.M72	6C4 21D5
	=PP1V25_S0_NB_PLL - @m72_lib.M72	6C4 21B4
	=PP1V25_S0M_NB_VCC - @m72_lib.M72	6C4 21A8
	=PP1V25_S0M_NB_VCCA - @m72_lib.M72	6C4 21B8
	=PP1V25_S0_NB_VCCDMI - @m72_lib.M72	6C4 19C3 21A8
	PP1V25_S0 - @m72_lib.M72	6C6 7D3 74C8
	=PP1V25_S0_SB_DMI - @m72_lib.M72	6C4 26C3 27C1
	=PP1V25_S0_NB_VCCDMI - @m72_lib.M72	6C4 19C3 21A8
	=PP1V25_S0_NB_VCC - @m72_lib.M72	6C4 21D5
	=PP1V25_S0_NB_PLL - @m72_lib.M72	6C4 21B4
	=PP1V25_S0M_NB_VCCA - @m72_lib.M72	6C4 21B8
	=PP1V25_S0M_NB_VCC - @m72_lib.M72	6C4 21A8
=PP2V5_S0_MXM	=PP2V5_S0_MXM - @m72_lib.M72	6D4 85A3
	PP2V5_S0 - @m72_lib.M72	6D6 7D3 77B2
=PP3V3_ENET_PHY	=PP3V3_ENET_PHY - @m72_lib.M72	37D6 38D6
	=PP3V3_S3_ENET - @m72_lib.M72	6D3 38B8 38D8 39A8
	=PP3V3_S3_BT - @m72_lib.M72	6D3 47D3
	=PP3V3_S3_MINI - @m72_lib.M72	6D3 34D2
	PP3V3_S3 - @m72_lib.M72	6A7 6D4 7D3 70D2 75D7 76B8 78C6
	=PP3V3_S3_MINI - @m72_lib.M72	6D3 34D2
	=PP3V3_S3_ENET - @m72_lib.M72	6D3 38B8 38D8 39A8
	=PP3V3_S3_BT - @m72_lib.M72	6D3 47D3
=PP3V3_S5_FAN	=PP3V3_S5_FAN - @m72_lib.M72	6D1 56B7 56D7 57D7
	=PP3V3_S5_SMBUS_SMC_A_S5 - @m72_lib.M72	6D1 52D3
	PP3V3_S5 - @m72_lib.M72	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @m72_lib.M72	6D1 46D5
	=PP3V3_S5_SMBUS_SMC_BSA - @m72_lib.M72	6D1 52C3
	=PP3V3_S5_LPCPLUS - @m72_lib.M72	6D1 7D4 51C6
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @m72_lib.M72	6D1 26B3 27B4
	=PP3V3_S5_SB_CLINK1 - @m72_lib.M72	6D1 25B1
	=PP3V3_S5_SB_GPIO - @m72_lib.M72	6D1 25D8
	=PP3V3_S5_ROM - @m72_lib.M72	6D1 61C6
	=PP3V3_S5_SMC - @m72_lib.M72	6D1 49D4 50B1 50D7
	=PP3V3_S5_FW - @m72_lib.M72	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
	=PP3V3_S5_SMBUS_SB_ME - @m72_lib.M72	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m72_lib.M72	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @m72_lib.M72	6D1 26A3 27D5
	=PP3V3_S5_SB_PM - @m72_lib.M72	6D1 28A5
	=PP3V3_S5_SB_USB - @m72_lib.M72	6D1 24C8
	=PP3V3_S5_SB - @m72_lib.M72	6D1 25A3 25A8 27D8 28D7
	PP3V3_S5 - @m72_lib.M72	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @m72_lib.M72	6D1 46D5
	=PP3V3_S5_SMC - @m72_lib.M72	6D1 49D4 50B1 50D7
	=PP3V3_S5_SMBUS_SMC_BSA - @m72_lib.M72	6D1 52C3
	=PP3V3_S5_SMBUS_SMC_A_S5 - @m72_lib.M72	6D1 52D3
	=PP3V3_S5_SMBUS_SB_ME - @m72_lib.M72	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m72_lib.M72	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @m72_lib.M72	6D1 26A3 27D5
	=PP3V3_S5_SB_USB - @m72_lib.M72	6D1 24C8
	=PP3V3_S5_SB_PM - @m72_lib.M72	6D1 28A5
	=PP3V3_S5_SB_GPIO - @m72_lib.M72	6D1 25D8
	=PP3V3_S5_SB_CLINK1 - @m72_lib.M72	6D1 25B1
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @m72_lib.M72	6D1 26B3 27B4
	=PP3V3_S5_SB - @m72_lib.M72	6D1 25A3 25A8 27D8 28D7
	=PP3V3_S5_ROM - @m72_lib.M72	6D1 61C6
	=PP3V3_S5_LPCPLUS - @m72_lib.M72	6D1 7D4 51C6
	=PP3V3_S5_FW - @m72_lib.M72	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @m72_lib.M72	6A4 98C4 98C6
	=PP5V_S0_MXM - @m72_lib.M72	6A4 84C7
	=PPV_S0_LCD_20INCH - @m72_lib.M72	6A4 90C8
	PP5V_S0 - @m72_lib.M72	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D3 94D6
	=PP5V_S0_SATA - @m72_lib.M72	6A4 6D6
	=PP5V_S0_LPCPLUS - @m72_lib.M72	6A4 7D4 51C6
	=PP5V_S0_PATA - @m72_lib.M72	6A4 44B6 44D6
	=PP5V_S0_SB - @m72_lib.M72	6A4 27D8
	PP5V_S0 - @m72_lib.M72	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D3 94D6
	=PPV_S0_LCD_20INCH - @m72_lib.M72	6A4 90C8
	=PP5V_S0_SB - @m72_lib.M72	6A4 27D8
	=PP5V_S0_PATA - @m72_lib.M72	6A4 44B6 44D6
	=PP5V_S0_MXM - @m72_lib.M72	6A4 84C7
	=PP5V_S0_LPCPLUS - @m72_lib.M72	6A4 7D4 51C6
=PP5V_S3_ALS	=PP5V_S3_ALS - @m72_lib.M72	6C3 58D5
	PP5V_S3 - @m72_lib.M72	6C4 7D3 70D3 75D8 76A8 78D6
	=PP5V_S3_SYSLED - @m72_lib.M72	6C3 50A5
	=PP5V_S3_MEMVTT - @m72_lib.M72	6C3 75B6
	=PP5V_S3_BNDI - @m72_lib.M72	6C3 47D7 58D5
	PP5V_S3 - @m72_lib.M72	6C4 7D3 70D3 75D8 76A8 78D6
	=PP5V_S3_SYSLED - @m72_lib.M72	6C3 50A5
	=PP5V_S3_MEMVTT - @m72_lib.M72	6C3 75B6
	=PP5V_S3_BNDI - @m72_lib.M72	6C3 47D7 58D5
=PP5V_S5_SB	=PP5V_S5_SB - @m72_lib.M72	6C1 27D8
	=PP5V_S5_USB - @m72_lib.M72	6C1 46C8 46D8
	PP5V_S5 - @m72_lib.M72	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78B7 78C2 78D6 78D8
	=PPVIN_S5_SMCVREF - @m72_lib.M72	6C1 50B8
	PP5V_S5 - @m72_lib.M72	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78B7 78C2 78D6 78D8
	=PPVIN_S5_SMCVREF - @m72_lib.M72	6C1 50B8
	=PP5V_S5_USB - @m72_lib.M72	6C1 46C8 46D8
=PP12V_S0_AUDIO_SPKRAMP	=PP12V_S0_AUDIO_SPKRAMP - @m72_lib.M72	6A4 98C6
	=PP12V_S0_CPU - @m72_lib.M72	6A4 53B8 71D8 72D7
	=PPV_S0_LCD_24INCH - @m72_lib.M72	6A4 90C8
	=PPV_S0_MXM_PWRSRC - @m72_lib.M72	6A4 53C4
	PP12V_S0 - @m72_lib.M72	6A6 6D8 7D3 73D7 74D7 76D8
	=PP12V_S0_FAN - @m72_lib.M72	6A4 56B6 56D7 57D6
	PP12V_S0 - @m72_lib.M72	6A6 6D8 7D3 73D7 74D7 76D8
	=PPV_S0_MXM_PWRSRC - @m72_lib.M72	6A4 53C4
	=PPV_S0_LCD_24INCH - @m72_lib.M72	6A4 90C8
	=PP12V_S0_FAN - @m72_lib.M72	6A4 56B6 56D7 57D6
	=PP12V_S0_CPU - @m72_lib.M72	6A4 53B8 71D8 72D7
=PP12V_S5_FET	=PP12V_S5_FET - @m72_lib.M72	6C1 78D3
	PP12V_S5 - @m72_lib.M72	6C2 6D6 7C3 70D8 76A8 76D5 78B7
	=PP12V_S5_FW - @m72_lib.M72	6C1 43D8
	PP12V_S5 - @m72_lib.M72	6C2 6D6 7C3 70D8 76A8 76D5 78B7
	=PP12V_S5_FW - @m72_lib.M72	6C1 43D8
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @m72_lib.M72	6D4 11B5 11D6 12D7 53B6 53D8
	PPVCORE_CPU - @m72_lib.M72	6D6 7D3 71D1 72C1
=SB_CLINK_MPWROK	=SB_CLINK_MPWROK - @m72_lib.M72	25C3 28B7
	PM_SB_PWROK - @m72_lib.M72	7C4 7C4 25C3 28B6 70C1
=SMC_SMS_INT	=SMC_SMS_INT - @m72_lib.M72	49B5 50B2
	SMC_SMS_INT - @m72_lib.M72	50B2
ACDC_TEMP	ACDC_TEMP - @m72_lib.M72	6D6 50C2
	SMC_ANALOG_ID - @m72_lib.M72	49A8 50C3
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @m72_lib.M72	7C4 7C4 49D8 50C2 70C1 84C7
	PM_LAN_PWRGD - @m72_lib.M72	49C5 50C3
ALS_GAIN	ALS_GAIN - @m72_lib.M72	49A5 50D5
	NC_ALS_GAIN - @m72_lib.M72	50D3
ALS_LEFT	ALS_LEFT - @m72_lib.M72	49A8 50D5
	TP_ALS_LEFT - @m72_lib.M72	50D3
ALS_RIGHT	ALS_RIGHT - @m72_lib.M72	49A8 58C4
ARB_DETECT_L	ARB_DETECT_L - @m72_lib.M72	25A7 25B3
CK505_48M_FSA	CK505_48M_FSA - @m72_lib.M72	29A3 30C8 105D3
CK505_CLKREQ1_L	CK505_CLKREQ1_L - @m72_lib.M72	29B3 30D2 85C8
CK505_CLKREQ3_L	CK505_CLKREQ3_L - @m72_lib.M72	29B3 30D2 40C3
CK505_CLKREQ6_L	CK505_CLKREQ6_L - @m72_lib.M72	29B3 30C2
	MINI_CLKREQ_L - @m72_lib.M72	30C2 34C6
CK505_CLKREQ8_L	CK505_CLKREQ8_L - @m72_lib.M72	29A3 30C2
	ENET_CLKREQ_L - @m72_lib.M72	30C2 38D3
CK505_CPU0_N	CK505_CPU0_N - @m72_lib.M72	29C3 30D5 105D3
	FSB_CLK_CPU_N - @m72_lib.M72	7C8 10B6 30D3 105C3
CK505_CPU0_P	CK505_CPU0_P - @m72_lib.M72	29C3 30D5 105D3
	FSB_CLK_CPU_P - @m72_lib.M72	7C8 10B6 30D3 105C3
CK505_CPU1_N	CK505_CPU1_N - @m72_lib.M72	29C3 30D5 105D3
	FSB_CLK_NB_N - @m72_lib.M72	7C3 7C7 14B3 30D3 105C3
CK505_CPU1_P	CK505_CPU1_P - @m72_lib.M72	29C3 30D5 105D3
	FSB_CLK_NB_P - @m72_lib.M72	7C7 14B3 30D3 105C3
CK505_CPU2_ITP_SRC10_N	CK505_CPU2_ITP_SRC10_N - @m72_lib.M72	29C3 30D5 105D3
	XDP_CLK_N - @m72_lib.M72	13B3 30D3 100A3 105C3
CK505_CPU2_ITP_SRC10_P	CK505_CPU2_ITP_SRC10_P - @m72_lib.M72	29C3 30D5 105D3
	XDP_CLK_P - @m72_lib.M72	13C3 30D3 100A3 105C3
CK505_DOT96_27M_N	CK505_DOT96_27M_N - @m72_lib.M72	29A3 30A5 105D3
	TP_CK505_27M_N - @m72_lib.M72	30A3
CK505_DOT96_27M_P	CK505_DOT96_27M_P - @m72_lib.M72	29A3 30A5 105D3
	TP_CK505_27M_P - @m72_lib.M72	30A3
CK505_FSA	CK505_FSA - @m72_lib.M72	30C7 105B3
CK505_FSB_TEST_MODE	CK505_FSB_TEST_MODE - @m72_lib.M72	29C5 30B8
CK505_FSC	CK505_FSC - @m72_lib.M72	30B7 105B3
CK505_LVDS_N	CK505_LVDS_N - @m72_lib.M72	29C3 30C5 105C3
	TP_CK505_LVDS_N - @m72_lib.M72	30C3

CK505_LVDS_P	CK505_LVDS_P - @m72_lib.M72	29B3 30C5 105D3
	TP_CK505_LVDS_P - @m72_lib.M72	30C3
CK505_PCI1_CLK	CK505_PCI1_CLK - @m72_lib.M72	29C5 30A5 105D3
	TP_CK505_PCI1_CLK - @m72_lib.M72	7C3 30A3
CK505_PCI2_CLK	CK505_PCI2_CLK - @m72_lib.M72	29B5 30A5 105D3
	TP_PCI_CLK33M_TPM - @m72_lib.M72	30A3
CK505_PCI3_CLK	CK505_PCI3_CLK - @m72_lib.M72	29B5 30A5 105D3
CK505_PCI4_CLK	CK505_PCI4_CLK - @m72_lib.M72	29B5 30A5 105D3
	TP_CK505_PCI4_CLK - @m72_lib.M72	30A3
CK505_PCI5_CLK_FCTSEL	CK505_PCI5_CLK_FCTSEL - @m72_lib.M72	29B5 30D8 105D3
CK505_PCIF0_CLK_ITPEN	CK505_PCIF0_CLK_ITPEN - @m72_lib.M72	29B7 30A5 105D3
CK505_PCIF1_CLK	CK505_PCIF1_CLK - @m72_lib.M72	29B5 30A5 105D3
CK505_REF0_FSC	CK505_REF0_FSC - @m72_lib.M72	29A3 30A8 105D3
CK505_REF1	CK505_REF1 - @m72_lib.M72	29A3 30B2
	TP_CK505_REF1 - @m72_lib.M72	7C3 30B1
CK505_SRC1_N	CK505_SRC1_N - @m72_lib.M72	29B3 30C5 105C3
	GPU_CLK100M_PCIE_N - @m72_lib.M72	30C3 85C7 105B3
CK505_SRC1_P	CK505_SRC1_P - @m72_lib.M72	29B3 30C5 105C3
	GPU_CLK100M_PCIE_P - @m72_lib.M72	30C3 85C7 105B3
CK505_SRC2_N	CK505_SRC2_N - @m72_lib.M72	29B3 30C5 105C3
	SB_CLK100M_DMI_N - @m72_lib.M72	7B8 7C3 24D2 30C3 105B3
CK505_SRC2_P	CK505_SRC2_P - @m72_lib.M72	29B3 30C5 105C3
	SB_CLK100M_DMI_P - @m72_lib.M72	7B3 7B8 24C2 30C3 105B3
CK505_SRC3_N	CK505_SRC3_N - @m72_lib.M72	29B3 30C5 105C3
	PCIE_CLK100M_FW_N - @m72_lib.M72	7D6 30C3 40C3 105B3
CK505_SRC3_P	CK505_SRC3_P - @m72_lib.M72	29B3 30C5 105C3
	PCIE_CLK100M_FW_P - @m72_lib.M72	7D6 30C3 40C3 105B3
CK505_SRC4_N	CK505_SRC4_N - @m72_lib.M72	29B3 30B5 105C3
	SB_CLK100M_SATA_N - @m72_lib.M72	7C8 23B6 30B3 105B3
CK505_SRC4_P	CK505_SRC4_P - @m72_lib.M72	29B3 30B5 105C3
	SB_CLK100M_SATA_P - @m72_lib.M72	7C8 23B6 30B3 105B3
CK505_SRC5_N	CK505_SRC5_N - @m72_lib.M72	29B3 30B5 105C3
	NB_CLK100M_PCIE_N - @m72_lib.M72	7C3 7C7 16C3 30B3 105B3
CK505_SRC5_P	CK505_SRC5_P - @m72_lib.M72	29B3 30B5 105C3
	NB_CLK100M_PCIE_P - @m72_lib.M72	7C7 16C3 30B3 105B3
CK505_SRC6_N	CK505_SRC6_N - @m72_lib.M72	29B3 30B5 105C3
	PCIE_CLK100M_MINI_N - @m72_lib.M72	30B3 34C6 105B3
CK505_SRC6_P	CK505_SRC6_P - @m72_lib.M72	29B3 30B5 105C3
	PCIE_CLK100M_MINI_P - @m72_lib.M72	30B3 34C6 105B3
CK505_SRC7_N	CK505_SRC7_N - @m72_lib.M72	29B3 30B5 105C3
CK505_SRC7_P	CK505_SRC7_P - @m72_lib.M72	29B3 30B5 105C3
CK505_SRC8_N	CK505_SRC8_N - @m72_lib.M72	29B3 30B5 105C3
	PCIE_CLK100M_ENET_N - @m72_lib.M72	7D6 30B3 37C8 105B3
CK505_SRC8_P	CK505_SRC8_P - @m72_lib.M72	29A3 30B5 105C3
	PCIE_CLK100M_ENET_P - @m72_lib.M72	7D6 30B3 37C8 105B3
CK505_XTAL_IN	CK505_XTAL_IN - @m72_lib.M72	29C5
CK505_XTAL_OUT	CK505_XTAL_OUT - @m72_lib.M72	29C5
CLINK_NB_CLK	CLINK_NB_CLK - @m72_lib.M72	7A7 7A8 16A3 25C3 104B3
CLINK_NB_DATA	CLINK_NB_DATA - @m72_lib.M72	7A7 7A8 16A3 25C3 104B3
CLINK_NB_RESET_L	CLINK_NB_RESET_L - @m72_lib.M72	16A3 25C3 104B3
CLINK_WLAN_CLK	CLINK_WLAN_CLK - @m72_lib.M72	34A8
	TP_CLINK_WLAN_CLK - @m72_lib.M72	25C3 34A6
CLINK_WLAN_DATA	CLINK_WLAN_DATA - @m72_lib.M72	34A8
	TP_CLINK_WLAN_DATA - @m72_lib.M72	7D2 25C3 28C4 34A6
CLINK_WLAN_RESET_L	CLINK_WLAN_RESET_L - @m72_lib.M72	34A8
	TP_CLINK_WLAN_RESET_L - @m72_lib.M72	25D5 34A6
CLK_PWRGD	CLK_PWRGD - @m72_lib.M72	25C3 29A3
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @m72_lib.M72	53B6
CPUVSENSE_IN	CPUVSENSE_IN - @m72_lib.M72	53D7
CPU_A20M_L	CPU_A20M_L - @m72_lib.M72	7C8 10C8 23C4 100B3
CPU_BSEL<0>	CPU_BSEL<0> - @m72_lib.M72	10B4 30C6 100B3
CPU_BSEL<1>	CPU_BSEL<1> - @m72_lib.M72	10A4 30B6 100B3
CPU_BSEL<2>	CPU_BSEL<2> - @m72_lib.M72	10A4 30B6 100A3
CPU_COMP<0>	CPU_COMP<0> - @m72_lib.M72	10B3 100A3
CPU_COMP<1>	CPU_COMP<1> - @m72_lib.M72	10B3 100A3
CPU_COMP<2>	CPU_COMP<2> - @m72_lib.M72	10B3 100A3
CPU_COMP<3>	CPU_COMP<3> - @m72_lib.M72	10B3 100A3
CPU_DPRSTP_L	CPU_DPRSTP_L - @m72_lib.M72	10B2 16B6 23C4 71C7 100A3
CPU_DPSLP_L	CPU_DPSLP_L - @m72_lib.M72	10B2 23C4 100B3
CPU_FERR_L	CPU_FERR_L - @m72_lib.M72	10C8 23C2 100B3
CPU_GTLREF	CPU_GTLREF - @m72_lib.M72	10B4 100A3
CPU_HSK_THRMD_N	CPU_HSK_THRMD_N - @m72_lib.M72	55A5 55A7 108A3
CPU_HSK_THRMD_P	CPU_HSK_THRMD_P - @m72_lib.M72	55A7 55B5 108A3
CPU_IERR_L	CPU_IERR_L - @m72_lib.M72	10D6 100B3
CPU_IGNNE_L	CPU_IGNNE_L - @m72_lib.M72	7C8 10C8 23C4 100B3
CPU_INIT_L	CPU_INIT_L - @m72_lib.M72	7C8 10D6 23C4 51B2 100B3
CPU_INIT_LS3V3	CPU_INIT_LS3V3 - @m72_lib.M72	51C4
CPU_INIT_R_L	CPU_INIT_R_L - @m72_lib.M72	51B3
CPU_INTR	CPU_INTR - @m72_lib.M72	7C8 10B8 23C4 100B3
CPU_NMI	CPU_NMI - @m72_lib.M72	7C8 10B8 23C4 100B3
CPU_PROCHOT_BUF	CPU_PROCHOT_BUF - @m72_lib.M72	50D2
CPU_PROCHOT_L	CPU_PROCHOT_L - @m72_lib.M72	10C5 50D3 100B3
CPU_PROCHOT_L_R	CPU_PROCHOT_L_R - @m72_lib.M72	50D2
CPU_PSI_L	CPU_PSI_L - @m72_lib.M72	10A2 28B7
	IMVP6_PSI_L - @m72_lib.M72	28B6 71C7
CPU_PWRGD	CPU_PWRGD - @m72_lib.M72	7C4 10B2 13C7 23C4 100B3
CPU_SMI_L	CPU_SMI_L - @m72_lib.M72	7C8 10B8 23C4 100B3
CPU_STPCLK_L	CPU_STPCLK_L - @m72_lib.M72	7C8 10B8 23C4 100B3
CPU_TEST1	CPU_TEST1 - @m72_lib.M72	10B4
CPU_TEST2	CPU_TEST2 - @m72_lib.M72	10B4
CPU_TEST4	CPU_TEST4 - @m72_lib.M72	10B4
CPU_THERMD_N	CPU_THERMD_N - @m72_lib.M72	10C6 55C5 108A3
CPU_THERMD_P	CPU_THERMD_P - @m72_lib.M72	10C6 55C5 108A3
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m72_lib.M72	23C4
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m72_lib.M72	11A5 71A3 100A3
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m72_lib.M72	11A5 71A3 100A3
CPU_VID<0>	CPU_VID<0> - @m72_lib.M72	11B6 12C2
CPU_VID<6..0>	CPU_VID<6..0> - @m72_lib.M72	100A3
CPU_VID<1>	CPU_VID<1> - @m72_lib.M72	11B6 12C2
CPU_VID<2>	CPU_VID<2> - @m72_lib.M72	11B6 12C2
CPU_VID<3>	CPU_VID<3> - @m72_lib.M72	11B6 12C2
CPU_VID<4>	CPU_VID<4> - @m72_lib.M72	11B6 12C2
CPU_VID<5>	CPU_VID<5> - @m72_lib.M72	11B6 12C2
CPU_VID<6>	CPU_VID<6> - @m72_lib.M72	11B6 12C2
DEBUG_RESET_L	DEBUG_RESET_L - @m72_lib.M72	7D4 28D1 51B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @m72_lib.M72	24C3
DMI_N2S_N<0>	DMI_N2S_N<0> - @m72_lib.M72	7B8 16B3 24D2
DMI_N2S_N<3..0>	DMI_N2S_N<3..0> - @m72_lib.M72	101D3
DMI_N2S_N<1>	DMI_N2S_N<1> - @m72_lib.M72	16B3 24D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @m72_lib.M72	16B3 24D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @m72_lib.M72	16B3 24D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @m72_lib.M72	7B8 16B3 24D2 101D3
DMI_N2S_P<1>	DMI_N2S_P<1> - @m72_lib.M72	16B3 24D2
DMI_N2S_P<3..1>	DMI_N2S_P<3..1> - @m72_lib.M72	101D3
DMI_N2S_P<2>	DMI_N2S_P<2> - @m72_lib.M72	16B3 24D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @m72_lib.M72	16B3 24D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @m72_lib.M72	7C7 16C3 24D2
DMI_S2N_N<3..0>	DMI_S2N_N<3..0> - @m72_lib.M72	101C3
DMI_S2N_N<1>	DMI_S2N_N<1> - @m72_lib.M72	16C3 24D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @m72_lib.M72	16B3 24D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @m72_lib.M72	16B3 24D2

DMI_S2N_P<0>	DMI_S2N_P<0> - @m72_lib.M72	7C7 16B3 24D2 101C3
DMI_S2N_P<1>	DMI_S2N_P<1> - @m72_lib.M72	16B3 24D2
DMI_S2N_P<3..1>	DMI_S2N_P<3..1> - @m72_lib.M72	101D3
DMI_S2N_P<2>	DMI_S2N_P<2> - @m72_lib.M72	16B3 24D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @m72_lib.M72	16B3 24D2
DVI_DDC_CLK	DVI_DDC_CLK - @m72_lib.M72	94D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @m72_lib.M72	94D3 94D5
DVI_DDC_DATA	DVI_DDC_DATA - @m72_lib.M72	94C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @m72_lib.M72	94C3 94D5
DVI_HOTPLUG_DET	DVI_HOTPLUG_DET - @m72_lib.M72	24A6 28B2
	SB_GPIO4 - @m72_lib.M72	28B2
DVI_HPD_UF	DVI_HPD_UF - @m72_lib.M72	94C3 94D5
ENET_CLK25M_XTALI	ENET_CLK25M_XTALI - @m72_lib.M72	7B3 37B4
ENET_CLK25M_XTALO	ENET_CLK25M_XTALO - @m72_lib.M72	7B3 37B4
ENET_CTAP_COMMON	ENET_CTAP_COMMON - @m72_lib.M72	39A4
ENET_CTRL12	ENET_CTRL12 - @m72_lib.M72	38A5 38B1
	TP_YUKON_CTRL12 - @m72_lib.M72	37C2 38B3
ENET_CTRL19R25	ENET_CTRL19R25 - @m72_lib.M72	38B1 38C6
	TP_YUKON_CTRL18 - @m72_lib.M72	37C2 38B3
ENET_LED_ACT_L	ENET_LED_ACT_L - @m72_lib.M72	37B2 39A8
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m72_lib.M72	37B2 39A8
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m72_lib.M72	37B2 39A8
ENET_LED_LINK_L	ENET_LED_LINK_L - @m72_lib.M72	37B2 39A8
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m72_lib.M72	37C2
ENET_MDI0	ENET_MDI0 - @m72_lib.M72	37B7 104B3
ENET_MDI1	ENET_MDI1 - @m72_lib.M72	37B6 104B3
ENET_MDI2	ENET_MDI2 - @m72_lib.M72	37B6 104B3
ENET_MDI3	ENET_MDI3 - @m72_lib.M72	37B5 104B3
ENET_MDI_N<0>	ENET_MDI_N<0> - @m72_lib.M72	37B8 39C7 104B3
ENET_MDI_N<1>	ENET_MDI_N<1> - @m72_lib.M72	37B8 39C7 104B3
ENET_MDI_N<2>	ENET_MDI_N<2> - @m72_lib.M72	37B8 39B7 104A3
ENET_MDI_N<3>	ENET_MDI_N<3> - @m72_lib.M72	37B8 39B7 104A3
ENET_MDI_P<0>	ENET_MDI_P<0> - @m72_lib.M72	37B8 39C7 104B3
ENET_MDI_P<1>	ENET_MDI_P<1> - @m72_lib.M72	37B8 39C7 104B3
ENET_MDI_P<2>	ENET_MDI_P<2> - @m72_lib.M72	37B8 39B7 104B3
ENET_MDI_P<3>	ENET_MDI_P<3> - @m72_lib.M72	37B8 39B7 104A3
ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @m72_lib.M72	108B3
ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @m72_lib.M72	108B3
ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @m72_lib.M72	108B3
ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @m72_lib.M72	108B3
ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @m72_lib.M72	108B3
ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @m72_lib.M72	108B3
ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @m72_lib.M72	108B3
ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @m72_lib.M72	108B3
ENET_MDI_T_N<0>	ENET_MDI_T_N<0> - @m72_lib.M72	39C5 108B3
ENET_MDI_T_N<1>	ENET_MDI_T_N<1> - @m72_lib.M72	39C5 108B3
ENET_MDI_T_N<2>	ENET_MDI_T_N<2> - @m72_lib.M72	39B5 108B3
ENET_MDI_T_N<3>	ENET_MDI_T_N<3> - @m72_lib.M72	39B5 108B3
ENET_MDI_T_P<0>	ENET_MDI_T_P<0> - @m72_lib.M72	39C5 108B3
ENET_MDI_T_P<1>	ENET_MDI_T_P<1> - @m72_lib.M72	39C5 108B3
ENET_MDI_T_P<2>	ENET_MDI_T_P<2> - @m72_lib.M72	39B5 108B3
ENET_MDI_T_P<3>	ENET_MDI_T_P<3> - @m72_lib.M72	39B5 108B3
ENET_RESET_L	ENET_RESET_L - @m72_lib.M72	7D6 28C1 37B8
EXCARD_OC_L	EXCARD_OC_L - @m72_lib.M72	24C8
EXTGPU_LVDS_EN	EXTGPU_LVDS_EN - @m72_lib.M72	13C3 24C8
EXTGPU_PWR_EN	EXTGPU_PWR_EN - @m72_lib.M72	23C4 28A2
	TP_EXTGPU_PWR_EN - @m72_lib.M72	28A1
EXTGPU_RST_L	EXTGPU_RST_L - @m72_lib.M72	25A5 25C5 28A2
	TP_EXTGPU_RST_L - @m72_lib.M72	28A1
F0_GATESLOWDN	F0_GATESLOWDN - @m72_lib.M72	56D5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m72_lib.M72	56D6
F1_GATESLOWDN	F1_GATESLOWDN - @m72_lib.M72	56B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m72_lib.M72	56B6
F2_GATESLOWDN	F2_GATESLOWDN - @m72_lib.M72	57D4
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m72_lib.M72	57D5
FAN_0_PWR	FAN_0_PWR - @m72_lib.M72	56C4
FAN_1_PWR	FAN_1_PWR - @m72_lib.M72	56B3
FAN_2_PWR	FAN_2_PWR - @m72_lib.M72	57C3
FAN_TACH0	FAN_TACH0 - @m72_lib.M72	56C7
FAN_TACH1	FAN_TACH1 - @m72_lib.M72	56A7
FAN_TACH2	FAN_TACH2 - @m72_lib.M72	57C7
FSB_ADSTB_L<0>	FSB_ADSTB_L<0> - @m72_lib.M72	7D7 7D8 10D8 14C3 100C3
FSB_ADSTB_L<1>	FSB_ADSTB_L<1> - @m72_lib.M72	7D7 7D8 10C8 14C3 100B3
FSB_ADS_L	FSB_ADS_L - @m72_lib.M72	10D6 14C3 100D3
FSB_A_L<3>	FSB_A_L<3> - @m72_lib.M72	10D8 14D3
FSB_A_L<5..3>	FSB_A_L<5..3> - @m72_lib.M72	100C3
FSB_A_L<4>	FSB_A_L<4> - @m72_lib.M72	10D8 14D3
FSB_A_L<5>	FSB_A_L<5> - @m72_lib.M72	10D8 14D3
FSB_A_L<6>	FSB_A_L<6> - @m72_lib.M72	7D7 7D8 10D8 14D3 100C3
FSB_A_L<7>	FSB_A_L<7> - @m72_lib.M72	10D8 14D3
FSB_A_L<16..7>	FSB_A_L<16..7> - @m72_lib.M72	100C3
FSB_A_L<8>	FSB_A_L<8> - @m72_lib.M72	10D8 14D3
FSB_A_L<9>	FSB_A_L<9> - @m72_lib.M72	10D8 14D3
FSB_A_L<10>	FSB_A_L<10> - @m72_lib.M72	10D8 14D3
FSB_A_L<11>	FSB_A_L<11> - @m72_lib.M72	10D8 14D3
FSB_A_L<12>	FSB_A_L<12> - @m72_lib.M72	10D8 14D3
FSB_A_L<13>	FSB_A_L<13> - @m72_lib.M72	10D8 14D3
FSB_A_L<14>	FSB_A_L<14> - @m72_lib.M72	10D8 14D3
FSB_A_L<15>	FSB_A_L<15> - @m72_lib.M72	10D8 14D3
FSB_A_L<16>	FSB_A_L<16> - @m72_lib.M72	10D8 14C3
FSB_A_L<17>	FSB_A_L<17> - @m72_lib.M72	10C8 14C3
FSB_A_L<26..17>	FSB_A_L<26..17> - @m72_lib.M72	100B3
FSB_A_L<18>	FSB_A_L<18> - @m72_lib.M72	10C8 14C3
FSB_A_L<19>	FSB_A_L<19> - @m72_lib.M72	10C8 14C3
FSB_A_L<20>	FSB_A_L<20> - @m72_lib.M72	10C8 14C3
FSB_A_L<21>	FSB_A_L<21> - @m72_lib.M72	10C8 14C3
FSB_A_L<22>	FSB_A_L<22> - @m72_lib.M72	10C8 14C3
FSB_A_L<23>	FSB_A_L<23> - @m72_lib.M72	10C8 14C3
FSB_A_L<24>	FSB_A_L<24> - @m72_lib.M72	10C8 14C3
FSB_A_L<25>	FSB_A_L<25> - @m72_lib.M72	10C8 14C3
FSB_A_L<26>	FSB_A_L<26> - @m72_lib.M72	10C8 14C3
FSB_A_L<27>	FSB_A_L<27> - @m72_lib.M72	7D7 7D8 10C8 14C3 100B3
FSB_A_L<28>	FSB_A_L<28> - @m72_lib.M72	10C8 14C3
FSB_A_L<35..28>	FSB_A_L<35..28> - @m72_lib.M72	100B3
FSB_A_L<29>	FSB_A_L<29> - @m72_lib.M72	10C8 14C3
FSB_A_L<30>	FSB_A_L<30> - @m72_lib.M72	10C8 14C3
FSB_A_L<31>	FSB_A_L<31> - @m72_lib.M72	10C8 14C3
FSB_A_L<32>	FSB_A_L<32> - @m72_lib.M72	10C8 14C3
FSB_A_L<33>	FSB_A_L<33> - @m72_lib.M72	10C8 14C3
FSB_A_L<34>	FSB_A_L<34> - @m72_lib.M72	10C8 14C3
FSB_A_L<35>	FSB_A_L<35> - @m72_lib.M72	10C8 14C3
FSB_BNR_L	FSB_BNR_L - @m72_lib.M72	7C7 10D6 14C3 100D3
FSB_BPRI_L	FSB_BPRI_L - @m72_lib.M72	10D6 14C3 100D3
FSB_BREQ0_L	FSB_BREQ0_L - @m72_lib.M72	7C7 10D6 14B3 100D3
FSB_CPURST_L	FSB_CPURST_L - @m72_lib.M72	7C8 10D6 13B2 14A5 100D3
FSB_CPUSLP_L	FSB_CPUSLP_L - @m72_lib.M72	10A2 14A5 100B3
FSB_DBSY_L	FSB_DBSY_L - @m72_lib.M72	7C7 10D6 14B3 100D3
FSB_DEFER_L	FSB_DEFER_L - @m72_lib.M72	10D6 14B3 100D3
FSB_DINV_L<0>	FSB_DINV_L<0> - @m72_lib.M72	7D7 7D8 10C4 14B3 100D3
FSB_DINV_L<1>	FSB_DINV_L<1> - @m72_lib.M72	7D7 7D8 10B4 14B3 100C3
FSB_DINV_L<2>	FSB_DINV_L<2> - @m72_lib.M72	7D7 7D8 10C2 14B3 100C3
FSB_DINV_L<3>	FSB_DINV_L<3> - @m72_lib.M72	7D7 7D8 10B2 14B3 100C3
FSB_DPWR_L	FSB_DPWR_L - @m72_lib.M72	7C7 10B2 14B3 100D3

FSB_DRDY_L	FSB_DRDY_L - @m72_lib.M72	10D6 14B3 100D3
FSB_DSTB_L_N<0>	FSB_DSTB_L_N<0> - @m72_lib.M72	7D7 7D8 10C4 14B3 100C3
FSB_DSTB_L_N<1>	FSB_DSTB_L_N<1> - @m72_lib.M72	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_N<2>	FSB_DSTB_L_N<2> - @m72_lib.M72	7D7 7D8 10C2 14B3 100C3
FSB_DSTB_L_N<3>	FSB_DSTB_L_N<3> - @m72_lib.M72	7D7 7D8 10B2 14B3 100C3
FSB_DSTB_L_P<0>	FSB_DSTB_L_P<0> - @m72_lib.M72	7D7 7D8 10C4 14B3 100D3
FSB_DSTB_L_P<1>	FSB_DSTB_L_P<1> - @m72_lib.M72	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_P<2>	FSB_DSTB_L_P<2> - @m72_lib.M72	7D7 7D8 10C2 14A3 100C3
FSB_DSTB_L_P<3>	FSB_DSTB_L_P<3> - @m72_lib.M72	7D7 7D8 10B2 14A3 100C3
FSB_D_L<0>	FSB_D_L<0> - @m72_lib.M72	7D7 7D8 10C4 14D5 100D3
FSB_D_L<1>	FSB_D_L<1> - @m72_lib.M72	10C4 14D5
FSB_D_L<15..1>	FSB_D_L<15..1> - @m72_lib.M72	100D3
FSB_D_L<2>	FSB_D_L<2> - @m72_lib.M72	10C4 14D5
FSB_D_L<3>	FSB_D_L<3> - @m72_lib.M72	10C4 14D5
FSB_D_L<4>	FSB_D_L<4> - @m72_lib.M72	10C4 14D5
FSB_D_L<5>	FSB_D_L<5> - @m72_lib.M72	10C4 14D5
FSB_D_L<6>	FSB_D_L<6> - @m72_lib.M72	10C4 14D5
FSB_D_L<7>	FSB_D_L<7> - @m72_lib.M72	10C4 14D5
FSB_D_L<8>	FSB_D_L<8> - @m72_lib.M72	10C4 14D5
FSB_D_L<9>	FSB_D_L<9> - @m72_lib.M72	10C4 14D5
FSB_D_L<10>	FSB_D_L<10> - @m72_lib.M72	10C4 14D5
FSB_D_L<11>	FSB_D_L<11> - @m72_lib.M72	10C4 14D5
FSB_D_L<12>	FSB_D_L<12> - @m72_lib.M72	10C4 14D5
FSB_D_L<13>	FSB_D_L<13> - @m72_lib.M72	10C4 14C5
FSB_D_L<14>	FSB_D_L<14> - @m72_lib.M72	10C4 14C5
FSB_D_L<15>	FSB_D_L<15> - @m72_lib.M72	10C4 14C5
FSB_D_L<16>	FSB_D_L<16> - @m72_lib.M72	7D7 7D8 10C4 14C5 100C3
FSB_D_L<17>	FSB_D_L<17> - @m72_lib.M72	10C4 14C5
FSB_D_L<31..17>	FSB_D_L<31..17> - @m72_lib.M72	100C3
FSB_D_L<18>	FSB_D_L<18> - @m72_lib.M72	10C4 14C5
FSB_D_L<19>	FSB_D_L<19> - @m72_lib.M72	10B4 14C5
FSB_D_L<20>	FSB_D_L<20> - @m72_lib.M72	10B4 14C5
FSB_D_L<21>	FSB_D_L<21> - @m72_lib.M72	10B4 14C5
FSB_D_L<22>	FSB_D_L<22> - @m72_lib.M72	10B4 14C5
FSB_D_L<23>	FSB_D_L<23> - @m72_lib.M72	10B4 14C5
FSB_D_L<24>	FSB_D_L<24> - @m72_lib.M72	10B4 14C5
FSB_D_L<25>	FSB_D_L<25> - @m72_lib.M72	10B4 14C5
FSB_D_L<26>	FSB_D_L<26> - @m72_lib.M72	10B4 14C5
FSB_D_L<27>	FSB_D_L<27> - @m72_lib.M72	10B4 14C5
FSB_D_L<28>	FSB_D_L<28> - @m72_lib.M72	10B4 14C5
FSB_D_L<29>	FSB_D_L<29> - @m72_lib.M72	10B4 14C5
FSB_D_L<30>	FSB_D_L<30> - @m72_lib.M72	10B4 14C5
FSB_D_L<31>	FSB_D_L<31> - @m72_lib.M72	10B4 14C5
FSB_D_L<32>	FSB_D_L<32> - @m72_lib.M72	10C2 14C5
FSB_D_L<40..32>	FSB_D_L<40..32> - @m72_lib.M72	100C3
FSB_D_L<33>	FSB_D_L<33> - @m72_lib.M72	10C2 14C5
FSB_D_L<34>	FSB_D_L<34> - @m72_lib.M72	10C2 14C5
FSB_D_L<35>	FSB_D_L<35> - @m72_lib.M72	10C2 14C5
FSB_D_L<36>	FSB_D_L<36> - @m72_lib.M72	10C2 14C5
FSB_D_L<37>	FSB_D_L<37> - @m72_lib.M72	10C2 14C5
FSB_D_L<38>	FSB_D_L<38> - @m72_lib.M72	10C2 14C5
FSB_D_L<39>	FSB_D_L<39> - @m72_lib.M72	10C2 14B5
FSB_D_L<40>	FSB_D_L<40> - @m72_lib.M72	10C2 14B5
FSB_D_L<41>	FSB_D_L<41> - @m72_lib.M72	7D7 7D8 10C2 14B5 100C3
FSB_D_L<42>	FSB_D_L<42> - @m72_lib.M72	10C2 14B5
FSB_D_L<47..42>	FSB_D_L<47..42> - @m72_lib.M72	100C3
FSB_D_L<43>	FSB_D_L<43> - @m72_lib.M72	10C2 14B5
FSB_D_L<44>	FSB_D_L<44> - @m72_lib.M72	10C2 14B5
FSB_D_L<45>	FSB_D_L<45> - @m72_lib.M72	10C2 14B5
FSB_D_L<46>	FSB_D_L<46> - @m72_lib.M72	10C2 14B5
FSB_D_L<47>	FSB_D_L<47> - @m72_lib.M72	10C2 14B5
FSB_D_L<48>	FSB_D_L<48> - @m72_lib.M72	10C2 14B5
FSB_D_L<58..48>	FSB_D_L<58..48> - @m72_lib.M72	100C3
FSB_D_L<49>	FSB_D_L<49> - @m72_lib.M72	10C2 14B5
FSB_D_L<50>	FSB_D_L<50> - @m72_lib.M72	10C2 14B5
FSB_D_L<51>	FSB_D_L<51> - @m72_lib.M72	10B2 14B5
FSB_D_L<52>	FSB_D_L<52> - @m72_lib.M72	10B2 14B5
FSB_D_L<53>	FSB_D_L<53> - @m72_lib.M72	10B2 14B5
FSB_D_L<54>	FSB_D_L<54> - @m72_lib.M72	10B2 14B5
FSB_D_L<55>	FSB_D_L<55> - @m72_lib.M72	10B2 14B5
FSB_D_L<56>	FSB_D_L<56> - @m72_lib.M72	10B2 14B5
FSB_D_L<57>	FSB_D_L<57> - @m72_lib.M72	10B2 14B5
FSB_D_L<58>	FSB_D_L<58> - @m72_lib.M72	10B2 14B5
FSB_D_L<59>	FSB_D_L<59> - @m72_lib.M72	7D7 7D8 10B2 14B5 100C3
FSB_D_L<60>	FSB_D_L<60> - @m72_lib.M72	10B2 14B5
FSB_D_L<63..60>	FSB_D_L<63..60> - @m72_lib.M72	100C3
FSB_D_L<61>	FSB_D_L<61> - @m72_lib.M72	10B2 14B5
FSB_D_L<62>	FSB_D_L<62> - @m72_lib.M72	10B2 14B5
FSB_D_L<63>	FSB_D_L<63> - @m72_lib.M72	10B2 14B5
FSB_HITM_L	FSB_HITM_L - @m72_lib.M72	7C7 10C6 14B3 100D3
FSB_HIT_L	FSB_HIT_L - @m72_lib.M72	7C7 10C6 14B3 100D3
FSB_LOCK_L	FSB_LOCK_L - @m72_lib.M72	7D7 7D8 10D6 14B3 100D3
FSB_REQ_L<0>	FSB_REQ_L<0> - @m72_lib.M72	7C7 7C8 10D8 14A3
FSB_REQ_L<4..0>	FSB_REQ_L<4..0> - @m72_lib.M72	100C3
FSB_REQ_L<1>	FSB_REQ_L<1> - @m72_lib.M72	7C7 7C8 10D8 14A3
FSB_REQ_L<2>	FSB_REQ_L<2> - @m72_lib.M72	7C7 7C8 10D8 14A3
FSB_REQ_L<3>	FSB_REQ_L<3> - @m72_lib.M72	7C7 7C8 10D8 14A3
FSB_REQ_L<4>	FSB_REQ_L<4> - @m72_lib.M72	7C7 7C8 10C8 14A3
FSB_RS_L<0>	FSB_RS_L<0> - @m72_lib.M72	10D6 14A3
FSB_RS_L<2..0>	FSB_RS_L<2..0> - @m72_lib.M72	100D3
FSB_RS_L<1>	FSB_RS_L<1> - @m72_lib.M72	10D6 14A3
FSB_RS_L<2>	FSB_RS_L<2> - @m72_lib.M72	10D6 14A3
FSB_TRDY_L	FSB_TRDY_L - @m72_lib.M72	10D6 14B3 100D3
FW643_REGCTL	FW643_REGCTL - @m72_lib.M72	40C3
FWH_INIT_L	FWH_INIT_L - @m72_lib.M72	7D4 51C5
FWH_MFG_MODE	FWH_MFG_MODE - @m72_lib.M72	25A7 25C5
FW_OCR10_CTL	FW_OCR10_CTL - @m72_lib.M72	40B6 42C8
FW_OCR10_CTL_R	FW_OCR10_CTL_R - @m72_lib.M72	42C7
FW_P0_TPA_C	FW_P0_TPA_C - @m72_lib.M72	43B8
FW_P0_TPBIAS	FW_P0_TPBIAS - @m72_lib.M72	40C6 43D8
FW_P1_TPA_C	FW_P1_TPA_C - @m72_lib.M72	43B7
FW_P1_TPBIAS	FW_P1_TPBIAS - @m72_lib.M72	40C6 43D8
FW_P2_TPA_N	FW_P2_TPA_N - @m72_lib.M72	40C6 43A8
	NC_FW_PORT2_TPA_N - @m72_lib.M72	43A6
FW_P2_TPA_P	FW_P2_TPA_P - @m72_lib.M72	40C6 43A8
	NC_FW_PORT2_TPA_P - @m72_lib.M72	43A6
FW_P2_TPBIAS	FW_P2_TPBIAS - @m72_lib.M72	40C6 43A8
	NC_FW_PORT2_TPBIAS - @m72_lib.M72	43A6
FW_P2_TPB_N	FW_P2_TPB_N - @m72_lib.M72	40C6 43A8
	NC_FW_PORT2_TPB_N - @m72_lib.M72	43A6
FW_P2_TPB_P	FW_P2_TPB_P - @m72_lib.M72	40C6 43A8
	NC_FW_PORT2_TPB_P - @m72_lib.M72	43A6
FW_PHY_DS0	FW_PHY_DS0 - @m72_lib.M72	40C6 42D3
FW_PHY_DS1	FW_PHY_DS1 - @m72_lib.M72	40C6 42D3
FW_PHY_DS2	FW_PHY_DS2 - @m72_lib.M72	40C6 42D3
FW_PORT0_TPA_N	FW_PORT0_TPA_N - @m72_lib.M72	43C5 43C6 106D3
	FW_P0_TPA_N - @m72_lib.M72	40C6 43C8
FW_PORT0_TPA_P	FW_PORT0_TPA_P - @m72_lib.M72	43C5 43C6 106D3
	FW_P0_TPA_P - @m72_lib.M72	40C6 43C8
FW_PORT0_TPA_R	FW_PORT0_TPA_R - @m72_lib.M72	43C2
FW_PORT0_TPB_N	FW_PORT0_TPB_N - @m72_lib.M72	43C5 43C6 106D3
	FW_P0_TPB_N - @m72_lib.M72	40C6 43C8
FW_PORT0_TPB_P	FW_PORT0_TPB_P - @m72_lib.M72	43C5 43C6 106D3
	FW_P0_TPB_P - @m72_lib.M72	40C6 43C8

FW_PORT0_VP	FW_PORT0_VP - @m72_lib.M72	43D3
FW_PORT0_VP_F	FW_PORT0_VP_F - @m72_lib.M72	43D5
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m72_lib.M72	43B2 106D3
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m72_lib.M72	43B2 106D3
FW_PORT1_TPA_N	FW_PORT1_TPA_N - @m72_lib.M72	43B6 43C6 106D3
	FW_P1_TPA_N - @m72_lib.M72	40C6 43C8
FW_PORT1_TPA_P	FW_PORT1_TPA_P - @m72_lib.M72	43B6 43C6 106D3
	FW_P1_TPA_P - @m72_lib.M72	40C6 43C8
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m72_lib.M72	43B2 106D3
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m72_lib.M72	43B2 106D3
FW_PORT1_TPB_N	FW_PORT1_TPB_N - @m72_lib.M72	43A6 43C6 106D3
	FW_P1_TPB_N - @m72_lib.M72	40C6 43C8
FW_PORT1_TPB_P	FW_PORT1_TPB_P - @m72_lib.M72	43B6 43C6 106D3
	FW_P1_TPB_P - @m72_lib.M72	40C6 43C8
FW_PORT1_VP	FW_PORT1_VP - @m72_lib.M72	43B3
FW_PORT1_VP_F	FW_PORT1_VP_F - @m72_lib.M72	43D5
FW_PORTS_VP	FW_PORTS_VP - @m72_lib.M72	43D7
FW_PORTS_VP_R	FW_PORTS_VP_R - @m72_lib.M72	40C7 43D6
FW_PU_RST_L	FW_PU_RST_L - @m72_lib.M72	40B6
FW_R0	FW_R0 - @m72_lib.M72	40B6
FW_RESET_L	FW_RESET_L - @m72_lib.M72	7B3 7D6 28C1 40B3
FW_REXT	FW_REXT - @m72_lib.M72	40B6
FW_SCL	FW_SCL - @m72_lib.M72	40B3
FW_TPCPS	FW_TPCPS - @m72_lib.M72	40B6
FW_TRST_L	FW_TRST_L - @m72_lib.M72	7C3 40C3
FW_VAUX_DETECT	FW_VAUX_DETECT - @m72_lib.M72	40C3
FW_XI	FW_XI - @m72_lib.M72	40B6
FW_XO	FW_XO - @m72_lib.M72	40B6
FW_XO_R	FW_XO_R - @m72_lib.M72	40B7
GATE_12V_S3	GATE_12V_S3 - @m72_lib.M72	78D2
GATE_12V_S3_R	GATE_12V_S3_R - @m72_lib.M72	78D3
GFX_VID<1>	GFX_VID<1> - @m72_lib.M72	16B3 22B8
GFX_VID<2>	GFX_VID<2> - @m72_lib.M72	16B3 22A8
GFX_VID<3>	GFX_VID<3> - @m72_lib.M72	16B3 22A8
GFX_VID<4>	GFX_VID<4> - @m72_lib.M72	16B3 22A8
GLAN_COMP	GLAN_COMP - @m72_lib.M72	23C6 104B3
GND_IMVP6_SGND	GND_IMVP6_SGND - @m72_lib.M72	71B6
GND_PP1V5REG_SGND	GND_PP1V5REG_SGND - @m72_lib.M72	73B7
GND_PP1V8REG_SGND	GND_PP1V8REG_SGND - @m72_lib.M72	75C5 75D6
GND_PP1V25REG_SGND	GND_PP1V25REG_SGND - @m72_lib.M72	74B7
GND_PP5VREG_SGND	GND_PP5VREG_SGND - @m72_lib.M72	76A7
GND_SMC_AVSS	GND_SMC_AVSS - @m72_lib.M72	49B2 50B7 53B2 53C6 53D2
		53D6 58C4
GPU_BLU	GPU_BLU - @m72_lib.M72	85C4 91B8 108B3
GPU_BUF_HSYNC	GPU_BUF_HSYNC - @m72_lib.M72	108A3
GPU_BUF_VSYNC	GPU_BUF_VSYNC - @m72_lib.M72	108A3
GPU_DDC_A_CLK	GPU_DDC_A_CLK - @m72_lib.M72	85C7 94D1
GPU_DDC_A_DATA	GPU_DDC_A_DATA - @m72_lib.M72	85C7 94C1
GPU_DDC_C_CLK	GPU_DDC_C_CLK - @m72_lib.M72	85A4 85C1 90A8
GPU_DDC_C_DATA	GPU_DDC_C_DATA - @m72_lib.M72	85A4 85D1 90A6
GPU_DIGON	GPU_DIGON - @m72_lib.M72	85A4 90B8
GPU_ENABLE_BL	GPU_ENABLE_BL - @m72_lib.M72	85A5
GPU_GRN	GPU_GRN - @m72_lib.M72	85C4 91B8 108B3
GPU_H2SYNC	GPU_H2SYNC - @m72_lib.M72	85C7 91A4 108B3
GPU_HPD	GPU_HPD - @m72_lib.M72	85A7 94C1
GPU_HSK_THRMD_N	GPU_HSK_THRMD_N - @m72_lib.M72	55A5 55A6 108A3
GPU_HSK_THRMD_P	GPU_HSK_THRMD_P - @m72_lib.M72	55A6 55B5 108A3
GPU_HSYNC_BUF	GPU_HSYNC_BUF - @m72_lib.M72	91A3
GPU_PRESENT	GPU_PRESENT - @m72_lib.M72	6A8 28C1
	SB_GPIO6 - @m72_lib.M72	25A5 25C5 28C2
GPU_PRESENT_DRAIN	GPU_PRESENT_DRAIN - @m72_lib.M72	6B7
GPU_PRESENT_R	GPU_PRESENT_R - @m72_lib.M72	6B7
GPU_RED	GPU_RED - @m72_lib.M72	85C4 91B8 108B3
GPU_TV_C	GPU_TV_C - @m72_lib.M72	85C4 91B8 108B3
GPU_TV_COMP	GPU_TV_COMP - @m72_lib.M72	85C4 91B8 108B3
GPU_TV_Y	GPU_TV_Y - @m72_lib.M72	85C4 91B8 108B3
GPU_V2SYNC	GPU_V2SYNC - @m72_lib.M72	85C7 91B4 108A3
GPU_VARY_BL	GPU_VARY_BL - @m72_lib.M72	85A4 90B3
GPU_VSYNC_BUF	GPU_VSYNC_BUF - @m72_lib.M72	91B3
HDA_BIT_CLK	HDA_BIT_CLK - @m72_lib.M72	23C8 98C6 103C3
HDA_BIT_CLK_R	HDA_BIT_CLK_R - @m72_lib.M72	23C6 103C3
HDA_DOCK_EN_L	HDA_DOCK_EN_L - @m72_lib.M72	23B6
HDA_RST_L	HDA_RST_L - @m72_lib.M72	23C8 98C6 103C3
HDA_RST_L_R	HDA_RST_L_R - @m72_lib.M72	23C6 103C3
HDA_SDIN0	HDA_SDIN0 - @m72_lib.M72	23C8 98C6 103B3
HDA_SDIN_CODEC	HDA_SDIN_CODEC - @m72_lib.M72	103B3
HDA_SDOUT	HDA_SDOUT - @m72_lib.M72	23B8 98C6 103B3
HDA_SDOUT_R	HDA_SDOUT_R - @m72_lib.M72	23B6 103B3
HDA_SYNC	HDA_SYNC - @m72_lib.M72	23C8 98C6 103C3
HDA_SYNC_R	HDA_SYNC_R - @m72_lib.M72	23C6 103C3
HDD_THRMD_N	HDD_THRMD_N - @m72_lib.M72	55A5 55B7 108A3
HDD_THRMD_P	HDD_THRMD_P - @m72_lib.M72	55B5 55B7 108A3
IDE_CSEL	IDE_CSEL - @m72_lib.M72	44B5
IDE_DASP_L	IDE_DASP_L - @m72_lib.M72	44B5
IDE_DASP_L_DS	IDE_DASP_L_DS - @m72_lib.M72	44B6
IDE_IOCS16_PU	IDE_IOCS16_PU - @m72_lib.M72	44C4
IDE_IRQ14	IDE_IRQ14 - @m72_lib.M72	23B4 44C6 103D3
IDE_PDA<0>	IDE_PDA<0> - @m72_lib.M72	23B4 44B5
IDE_PDA<2..0>	IDE_PDA<2..0> - @m72_lib.M72	103D3
IDE_PDA<1>	IDE_PDA<1> - @m72_lib.M72	23B4 44B5
IDE_PDA<2>	IDE_PDA<2> - @m72_lib.M72	23B4 44B4
IDE_PDCS1_L	IDE_PDCS1_L - @m72_lib.M72	23B4 44B5 103D3
IDE_PDCS3_L	IDE_PDCS3_L - @m72_lib.M72	23B4 44B4 103D3
IDE_PDD<0>	IDE_PDD<0> - @m72_lib.M72	23C4 44C5
IDE_PDD<8..0>	IDE_PDD<8..0> - @m72_lib.M72	103D3
IDE_PDD<1>	IDE_PDD<1> - @m72_lib.M72	23C4 44C5
IDE_PDD<2>	IDE_PDD<2> - @m72_lib.M72	23B4 44C5
IDE_PDD<3>	IDE_PDD<3> - @m72_lib.M72	23B4 44C5
IDE_PDD<4>	IDE_PDD<4> - @m72_lib.M72	23B4 44C5
IDE_PDD<5>	IDE_PDD<5> - @m72_lib.M72	23B4 44C5
IDE_PDD<6>	IDE_PDD<6> - @m72_lib.M72	23B4 44C5
IDE_PDD<7>	IDE_PDD<7> - @m72_lib.M72	23B4 44C5
IDE_PDD<8>	IDE_PDD<8> - @m72_lib.M72	23B4 44C4
IDE_PDD<9>	IDE_PDD<9> - @m72_lib.M72	7B8 23B4 44C4 103D3
IDE_PDD<10>	IDE_PDD<10> - @m72_lib.M72	23B4 44C4
IDE_PDD<15..10>	IDE_PDD<15..10> - @m72_lib.M72	103D3
IDE_PDD<11>	IDE_PDD<11> - @m72_lib.M72	23B4 44C4
IDE_PDD<12>	IDE_PDD<12> - @m72_lib.M72	23B4 44C4
IDE_PDD<13>	IDE_PDD<13> - @m72_lib.M72	23B4 44C4
IDE_PDD<14>	IDE_PDD<14> - @m72_lib.M72	23B4 44C4
IDE_PDD<15>	IDE_PDD<15> - @m72_lib.M72	23B4 44C4
IDE_PDDACK_L	IDE_PDDACK_L - @m72_lib.M72	23B4 44C4 103D3
IDE_PDDREQ	IDE_PDDREQ - @m72_lib.M72	23A4 44B6 103D3
IDE_PDIORDY	IDE_PDIORDY - @m72_lib.M72	7B8 23A4 44C6 103D3
IDE_PDIOR_L	IDE_PDIOR_L - @m72_lib.M72	7C8 23B4 44C4 103D3
IDE_PDIOW_L	IDE_PDIOW_L - @m72_lib.M72	23B4 44C5 103D3
IMVP6_BOOT1	IMVP6_BOOT1 - @m72_lib.M72	71A6 71D4
IMVP6_BOOT1_RC	IMVP6_BOOT1_RC - @m72_lib.M72	71A6 71D4
IMVP6_BOOT2	IMVP6_BOOT2 - @m72_lib.M72	71A4 71C4
IMVP6_BOOT2_RC	IMVP6_BOOT2_RC - @m72_lib.M72	71A4 71C4
IMVP6_BOOT3	IMVP6_BOOT3 - @m72_lib.M72	72A7 72C6
IMVP6_BOOT3_RC	IMVP6_BOOT3_RC - @m72_lib.M72	72A7 72C5
IMVP6_COMP	IMVP6_COMP - @m72_lib.M72	71A8 71B7
IMVP6_COMP_RC	IMVP6_COMP_RC - @m72_lib.M72	71B8

IMVP6_DFB	IMVP6_DFB - @m72_lib.M72	71A8 71B5
IMVP6_DROOP	IMVP6_DROOP - @m72_lib.M72	71A8 71B4
IMVP6_FB	IMVP6_FB - @m72_lib.M72	71A8 71B7
IMVP6_FCCM	IMVP6_FCCM - @m72_lib.M72	71A8 71C5 72C7
IMVP6_FET_RC1	IMVP6_FET_RC1 - @m72_lib.M72	71A6 71C3
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m72_lib.M72	71A4 71B3
IMVP6_FET_RC3	IMVP6_FET_RC3 - @m72_lib.M72	72A7 72C3
IMVP6_ISEN1	IMVP6_ISEN1 - @m72_lib.M72	71A6 71C3 72C1
IMVP6_ISEN2	IMVP6_ISEN2 - @m72_lib.M72	71A4 71C5
IMVP6_ISEN3	IMVP6_ISEN3 - @m72_lib.M72	71C5 72A7 72B1
IMVP6_LGATE1	IMVP6_LGATE1 - @m72_lib.M72	71A6 71D4
IMVP6_LGATE2	IMVP6_LGATE2 - @m72_lib.M72	71A4 71C4
IMVP6_LGATE3	IMVP6_LGATE3 - @m72_lib.M72	72A7 72C6
IMVP6_NTC	IMVP6_NTC - @m72_lib.M72	71C7
IMVP6_NTC_R	IMVP6_NTC_R - @m72_lib.M72	71C8
IMVP6_OCSET	IMVP6_OCSET - @m72_lib.M72	71A8 71B5
IMVP6_PHASE1	IMVP6_PHASE1 - @m72_lib.M72	71A6 71D4 108D1
IMVP6_PHASE2	IMVP6_PHASE2 - @m72_lib.M72	71A4 71C4 108D1
IMVP6_PHASE3	IMVP6_PHASE3 - @m72_lib.M72	72A7 72C6 108D1
IMVP6_PMON	IMVP6_PMON - @m72_lib.M72	53C8 71C5
IMVP6_PWM1	IMVP6_PWM1 - @m72_lib.M72	71A6 71D5
IMVP6_PWM2	IMVP6_PWM2 - @m72_lib.M72	71A4 71C5
IMVP6_PWM3	IMVP6_PWM3 - @m72_lib.M72	71C5 72A7 72C7
IMVP6_RBIAS	IMVP6_RBIAS - @m72_lib.M72	71A8 71B7
IMVP6_SOFT	IMVP6_SOFT - @m72_lib.M72	71A8 71C7
IMVP6_UGATE1	IMVP6_UGATE1 - @m72_lib.M72	71A6 71D4
IMVP6_UGATE2	IMVP6_UGATE2 - @m72_lib.M72	71A4 71C4
IMVP6_UGATE3	IMVP6_UGATE3 - @m72_lib.M72	72A7 72C6
IMVP6_VDIFF	IMVP6_VDIFF - @m72_lib.M72	71A8 71B7
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m72_lib.M72	71B8
IMVP6_VID<0>	IMVP6_VID<0> - @m72_lib.M72	12C1 71C7
IMVP6_VID<6..0>	IMVP6_VID<6..0> - @m72_lib.M72	100A3
IMVP6_VID<1>	IMVP6_VID<1> - @m72_lib.M72	12C1 71C7
IMVP6_VID<2>	IMVP6_VID<2> - @m72_lib.M72	12C1 71C7
IMVP6_VID<3>	IMVP6_VID<3> - @m72_lib.M72	12C1 71C7
IMVP6_VID<4>	IMVP6_VID<4> - @m72_lib.M72	12C1 71C7
IMVP6_VID<5>	IMVP6_VID<5> - @m72_lib.M72	12C1 71C7
IMVP6_VID<6>	IMVP6_VID<6> - @m72_lib.M72	12C1 71C7
IMVP6_VO	IMVP6_VO - @m72_lib.M72	71A8 71B4 72C1
IMVP6_VO1	IMVP6_VO1 - @m72_lib.M72	71A6 71D1
IMVP6_VO2	IMVP6_VO2 - @m72_lib.M72	71A4 71B1
IMVP6_VO3	IMVP6_VO3 - @m72_lib.M72	72A7 72C2
IMVP6_VO_R	IMVP6_VO_R - @m72_lib.M72	71B4
IMVP6_VR_TT_L	IMVP6_VR_TT_L - @m72_lib.M72	71C7
IMVP6_VSEN_N	IMVP6_VSEN_N - @m72_lib.M72	71A5 100A3
IMVP6_VSEN_P	IMVP6_VSEN_P - @m72_lib.M72	71A5 100A3
IMVP6_VSUM	IMVP6_VSUM - @m72_lib.M72	71A8 71C4 72B1
IMVP6_VSUM1	IMVP6_VSUM1 - @m72_lib.M72	71A6 71C2
IMVP6_VSUM2	IMVP6_VSUM2 - @m72_lib.M72	71A4 71B2
IMVP6_VSUM3	IMVP6_VSUM3 - @m72_lib.M72	72A7 72C3
IMVP6_VW	IMVP6_VW - @m72_lib.M72	71A8 71B7
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m72_lib.M72	71C7 100B3
IMVP_PGD_IN	IMVP_PGD_IN - @m72_lib.M72	70B3
IMVP_VR_ON	IMVP_VR_ON - @m72_lib.M72	7C4 49C8 71C7
INT_PIRQA_L	INT_PIRQA_L - @m72_lib.M72	24A4 24A8 104C3
INT_PIRQB_L	INT_PIRQB_L - @m72_lib.M72	24A4 24A8 104C3
INT_PIRQC_L	INT_PIRQC_L - @m72_lib.M72	24A4 24A8 104C3
INT_PIRQD_L	INT_PIRQD_L - @m72_lib.M72	24A4 24A8 104C3
INT_PIRQE_L	INT_PIRQE_L - @m72_lib.M72	24A4 24A6 104C3
INT_PIRQF_L	INT_PIRQF_L - @m72_lib.M72	24A4 24A6 104C3
INT_SERIRQ	INT_SERIRQ - @m72_lib.M72	7D4 25C8 49C8 51B4
INV_EN_BL_OR_PANEL_I D	INV_EN_BL_OR_PANEL_ID - @m72_lib.M72	6D6 28B2 85A3
ISENSE_CAL_EN	ISENSE_CAL_EN - @m72_lib.M72	49B8 50A2 53A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m72_lib.M72	53B8
ISENSE_CAL_EN_LS12V	ISENSE_CAL_EN_LS12V - @m72_lib.M72	53B7
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @m72_lib.M72	53B8
ITP_CPURST_L	ITP_CPURST_L - @m72_lib.M72	100A3
ITS_ALIVE	ITS_ALIVE - @m72_lib.M72	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @m72_lib.M72	6A8
LAN_ENERGY_DET	LAN_ENERGY_DET - @m72_lib.M72	23C6 28A2
	TP_LAN_ENERGY_DET - @m72_lib.M72	28A1
LAN_PHYPC	LAN_PHYPC - @m72_lib.M72	25A5 25C5
LCD_PWM	LCD_PWM - @m72_lib.M72	6D8 90B1
LCD_PWREN_DIV	LCD_PWREN_DIV - @m72_lib.M72	90C8
LCD_PWREN_L	LCD_PWREN_L - @m72_lib.M72	90B7
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @m72_lib.M72	90C7
LCD_SHOULD_ON	LCD_SHOULD_ON - @m72_lib.M72	6A6
LED4300_1	LED4300_1 - @m72_lib.M72	39A7
LED4301_1	LED4301_1 - @m72_lib.M72	39A7
LED4302_1	LED4302_1 - @m72_lib.M72	39A6
LED4303_1	LED4303_1 - @m72_lib.M72	39A6
LINDACARD_GPIO	LINDACARD_GPIO - @m72_lib.M72	7C4 25A7 25D5 51B4
LPC_AD<0>	LPC_AD<0> - @m72_lib.M72	7D4 23D4 49C8 51C6
LPC_AD<1>	LPC_AD<1> - @m72_lib.M72	7A8 7C6 7D4 23D4 49C8 51C6
LPC_AD<2>	LPC_AD<2> - @m72_lib.M72	7D4 23D4 49C8 51C4
LPC_AD<3>	LPC_AD<3> - @m72_lib.M72	7D4 23D4 49C8 51C4
LPC_FRAME_L	LPC_FRAME_L - @m72_lib.M72	7D4 23D4 49C8 51B6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m72_lib.M72	15C5 22D8
	TP_LVDS_A_CLK_N - @m72_lib.M72	22D7
LVDS_A_CLK_P	LVDS_A_CLK_P - @m72_lib.M72	15C5 22D8
	TP_LVDS_A_CLK_P - @m72_lib.M72	22D7
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m72_lib.M72	15C5 22D8
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m72_lib.M72	15C5 22C8
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m72_lib.M72	15C5 22C8
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m72_lib.M72	15C5 22C8
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m72_lib.M72	15C5 22C8
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m72_lib.M72	15C5 22C8
LVDS_BKLT_CTL	LVDS_BKLT_CTL - @m72_lib.M72	15D5 22D8
	TP_LVDS_BKLT_CTL - @m72_lib.M72	22D7
LVDS_BKLT_EN	LVDS_BKLT_EN - @m72_lib.M72	15D5 22D8
	TP_LVDS_BKLT_EN - @m72_lib.M72	7B3 22D7
LVDS_B_CLK_N	LVDS_B_CLK_N - @m72_lib.M72	15C5 22D8
	TP_LVDS_B_CLK_N - @m72_lib.M72	22D7
LVDS_B_CLK_P	LVDS_B_CLK_P - @m72_lib.M72	15C5 22D8
	TP_LVDS_B_CLK_P - @m72_lib.M72	22D7
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m72_lib.M72	15C5 22C8
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m72_lib.M72	15C5 22C8
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m72_lib.M72	15C5 22C8
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m72_lib.M72	15C5 22C8
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m72_lib.M72	15C5 22C8
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m72_lib.M72	15C5 22C8
LVDS_IBG	LVDS_IBG - @m72_lib.M72	15D5 22D8
	TP_LVDS_IBG - @m72_lib.M72	22D7
LVDS_L_CLK_N	LVDS_L_CLK_N - @m72_lib.M72	85B4 90A6 108C3
LVDS_L_CLK_P	LVDS_L_CLK_P - @m72_lib.M72	85B4 90A8 108C3
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @m72_lib.M72	85A4 90A6
LVDS_L_DATA_N<3..0>	LVDS_L_DATA_N<3..0> - @m72_lib.M72	108C3
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @m72_lib.M72	85B4 90A8
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @m72_lib.M72	85B4 90A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @m72_lib.M72	85B4 90A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @m72_lib.M72	85A4 90A8
LVDS_L_DATA_P<3..0>	LVDS_L_DATA_P<3..0> - @m72_lib.M72	108C3

LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @m72_lib.M72	85B4 90A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @m72_lib.M72	85B4 90A8
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @m72_lib.M72	85B4 90A8
LVDS_U_CLK_N	LVDS_U_CLK_N - @m72_lib.M72	85B4 90A6 108C3
LVDS_U_CLK_P	LVDS_U_CLK_P - @m72_lib.M72	85B4 90A8 108C3
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @m72_lib.M72	85B4 90A8
LVDS_U_DATA_N<3..0>	LVDS_U_DATA_N<3..0> - @m72_lib.M72	108C3
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @m72_lib.M72	85B4 90A8
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @m72_lib.M72	85B4 90A8
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @m72_lib.M72	85B4 90A6
LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @m72_lib.M72	85B4 90A6
LVDS_U_DATA_P<3..0>	LVDS_U_DATA_P<3..0> - @m72_lib.M72	108C3
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @m72_lib.M72	85B4 90A6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @m72_lib.M72	85B4 90A6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @m72_lib.M72	85B4 90A8
LVDS_VDD_EN	LVDS_VDD_EN - @m72_lib.M72	15D5 22D8
	TP_LVDS_VDD_EN - @m72_lib.M72	22D7
LVDS_VREFH	LVDS_VREFH - @m72_lib.M72	15D5 22D8
	TP_LVDS_VREFH - @m72_lib.M72	22D7
LVDS_VREFL	LVDS_VREFL - @m72_lib.M72	15D5 22D8
	TP_LVDS_VREFL - @m72_lib.M72	22D7
MCH_CORES0_BOOT	MCH_CORES0_BOOT - @m72_lib.M72	74C4
MCH_CORES0_BOOT_R	MCH_CORES0_BOOT_R - @m72_lib.M72	74C3
MCH_CORES0_ISEN	MCH_CORES0_ISEN - @m72_lib.M72	74C4
MCH_CORES0_LGATE	MCH_CORES0_LGATE - @m72_lib.M72	74C3
MCH_CORES0_OCSET	MCH_CORES0_OCSET - @m72_lib.M72	74B4
MCH_CORES0_SNUBBER_R	MCH_CORES0_SNUBBER_R - @m72_lib.M72	74C2
MCH_CORES0_SOFT	MCH_CORES0_SOFT - @m72_lib.M72	74C4
MCH_CORES0_SWITCHNOD E	MCH_CORES0_SWITCHNODE - @m72_lib.M72	74C3 108D1
MCH_CORES0_UGATE	MCH_CORES0_UGATE - @m72_lib.M72	74C4
MCH_CORES0_VSEN	MCH_CORES0_VSEN - @m72_lib.M72	74B3
MEMVTT_VREF	MEMVTT_VREF - @m72_lib.M72	75A4
MEM_A_A<0>	MEM_A_A<0> - @m72_lib.M72	17C5 31B3 33C6
MEM_A_A<14..0>	MEM_A_A<14..0> - @m72_lib.M72	102D3
MEM_A_A<1>	MEM_A_A<1> - @m72_lib.M72	17C5 31B6 33C6
MEM_A_A<2>	MEM_A_A<2> - @m72_lib.M72	17B5 31B3 33C6
MEM_A_A<3>	MEM_A_A<3> - @m72_lib.M72	17B5 31B6 33C6
MEM_A_A<4>	MEM_A_A<4> - @m72_lib.M72	17B5 31C3 33C6
MEM_A_A<5>	MEM_A_A<5> - @m72_lib.M72	17B5 31C6 33C6
MEM_A_A<6>	MEM_A_A<6> - @m72_lib.M72	17B5 31C3 33C6
MEM_A_A<7>	MEM_A_A<7> - @m72_lib.M72	17B5 31C3 33C6
MEM_A_A<8>	MEM_A_A<8> - @m72_lib.M72	17B5 31C6 33C6
MEM_A_A<9>	MEM_A_A<9> - @m72_lib.M72	17B5 31C6 33C6
MEM_A_A<10>	MEM_A_A<10> - @m72_lib.M72	17B5 31B6 33C6
MEM_A_A<11>	MEM_A_A<11> - @m72_lib.M72	17B5 31C3 33C6
MEM_A_A<12>	MEM_A_A<12> - @m72_lib.M72	17B5 31C6 33C6
MEM_A_A<13>	MEM_A_A<13> - @m72_lib.M72	17B5 31B3 33C6
MEM_A_A<14>	MEM_A_A<14> - @m72_lib.M72	16C6 31C3 33C6
MEM_A_BS<0>	MEM_A_BS<0> - @m72_lib.M72	17D5 31B6 33B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @m72_lib.M72	102D3
MEM_A_BS<1>	MEM_A_BS<1> - @m72_lib.M72	17D5 31B3 33B6
MEM_A_BS<2>	MEM_A_BS<2> - @m72_lib.M72	17D5 31C6 33B6
MEM_A_CAS_L	MEM_A_CAS_L - @m72_lib.M72	17D5 31B6 33B6 102D3
MEM_A_DM<0>	MEM_A_DM<0> - @m72_lib.M72	17D5 31D3 102C3
MEM_A_DM<1>	MEM_A_DM<1> - @m72_lib.M72	17D5 31D3 102C3
MEM_A_DM<2>	MEM_A_DM<2> - @m72_lib.M72	17C5 31C3 102C3
MEM_A_DM<3>	MEM_A_DM<3> - @m72_lib.M72	17C5 31C6 102C3
MEM_A_DM<4>	MEM_A_DM<4> - @m72_lib.M72	17C5 31B3 102C3
MEM_A_DM<5>	MEM_A_DM<5> - @m72_lib.M72	17C5 31B6 102C3
MEM_A_DM<6>	MEM_A_DM<6> - @m72_lib.M72	17C5 31A3 102C3
MEM_A_DM<7>	MEM_A_DM<7> - @m72_lib.M72	17C5 31A6 102C3
MEM_A_DQ<0>	MEM_A_DQ<0> - @m72_lib.M72	17D8 31D6
MEM_A_DQ<6..0>	MEM_A_DQ<6..0> - @m72_lib.M72	102D3
MEM_A_DQ<1>	MEM_A_DQ<1> - @m72_lib.M72	17D8 31D6
MEM_A_DQ<2>	MEM_A_DQ<2> - @m72_lib.M72	17D8 31D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @m72_lib.M72	17D8 31D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @m72_lib.M72	17D8 31D3
MEM_A_DQ<5>	MEM_A_DQ<5> - @m72_lib.M72	17D8 31D3
MEM_A_DQ<6>	MEM_A_DQ<6> - @m72_lib.M72	17D8 31D3
MEM_A_DQ<7>	MEM_A_DQ<7> - @m72_lib.M72	7C7 17D8 31D3 102D3
MEM_A_DQ<8>	MEM_A_DQ<8> - @m72_lib.M72	17C8 31D6
MEM_A_DQ<13..8>	MEM_A_DQ<13..8> - @m72_lib.M72	102D3
MEM_A_DQ<9>	MEM_A_DQ<9> - @m72_lib.M72	17C8 31D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @m72_lib.M72	17C8 31D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @m72_lib.M72	17C8 31D6
MEM_A_DQ<12>	MEM_A_DQ<12> - @m72_lib.M72	17C8 31D3
MEM_A_DQ<13>	MEM_A_DQ<13> - @m72_lib.M72	17C8 31D3
MEM_A_DQ<14>	MEM_A_DQ<14> - @m72_lib.M72	7C7 17C8 31D3 102D3
MEM_A_DQ<15>	MEM_A_DQ<15> - @m72_lib.M72	17C8 31D3 102C3
MEM_A_DQ<16>	MEM_A_DQ<16> - @m72_lib.M72	7B7 17C8 31D6 102C3
MEM_A_DQ<17>	MEM_A_DQ<17> - @m72_lib.M72	17C8 31D6
MEM_A_DQ<23..17>	MEM_A_DQ<23..17> - @m72_lib.M72	102C3
MEM_A_DQ<18>	MEM_A_DQ<18> - @m72_lib.M72	17C8 31C6
MEM_A_DQ<19>	MEM_A_DQ<19> - @m72_lib.M72	17C8 31C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @m72_lib.M72	17C8 31D3
MEM_A_DQ<21>	MEM_A_DQ<21> - @m72_lib.M72	17C8 31D3
MEM_A_DQ<22>	MEM_A_DQ<22> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<23>	MEM_A_DQ<23> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<24>	MEM_A_DQ<24> - @m72_lib.M72	17C8 31C6 102C3
MEM_A_DQ<25>	MEM_A_DQ<25> - @m72_lib.M72	7B7 17C8 31C6 102C3
MEM_A_DQ<26>	MEM_A_DQ<26> - @m72_lib.M72	17C8 31C6
MEM_A_DQ<31..26>	MEM_A_DQ<31..26> - @m72_lib.M72	102C3
MEM_A_DQ<27>	MEM_A_DQ<27> - @m72_lib.M72	17C8 31C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<29>	MEM_A_DQ<29> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<30>	MEM_A_DQ<30> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<31>	MEM_A_DQ<31> - @m72_lib.M72	17C8 31C3
MEM_A_DQ<32>	MEM_A_DQ<32> - @m72_lib.M72	17C8 31B6
MEM_A_DQ<38..32>	MEM_A_DQ<38..32> - @m72_lib.M72	102C3
MEM_A_DQ<33>	MEM_A_DQ<33> - @m72_lib.M72	17C8 31B6
MEM_A_DQ<34>	MEM_A_DQ<34> - @m72_lib.M72	17B8 31B6
MEM_A_DQ<35>	MEM_A_DQ<35> - @m72_lib.M72	17B8 31B6
MEM_A_DQ<36>	MEM_A_DQ<36> - @m72_lib.M72	17B8 31B3
MEM_A_DQ<37>	MEM_A_DQ<37> - @m72_lib.M72	17B8 31B3
MEM_A_DQ<38>	MEM_A_DQ<38> - @m72_lib.M72	17B8 31B3
MEM_A_DQ<39>	MEM_A_DQ<39> - @m72_lib.M72	7B7 17B8 31B3 102C3
MEM_A_DQ<40>	MEM_A_DQ<40> - @m72_lib.M72	17B8 31B6
MEM_A_DQ<46..40>	MEM_A_DQ<46..40> - @m72_lib.M72	102C3
MEM_A_DQ<41>	MEM_A_DQ<41> - @m72_lib.M72	17B8 31B6
MEM_A_DQ<42>	MEM_A_DQ<42> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<43>	MEM_A_DQ<43> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<44>	MEM_A_DQ<44> - @m72_lib.M72	17B8 31B3
MEM_A_DQ<45>	MEM_A_DQ<45> - @m72_lib.M72	17B8 31B3
MEM_A_DQ<46>	MEM_A_DQ<46> - @m72_lib.M72	17B8 31A3
MEM_A_DQ<47>	MEM_A_DQ<47> - @m72_lib.M72	7B7 17B8 31A3 102C3
MEM_A_DQ<48>	MEM_A_DQ<48> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<53..48>	MEM_A_DQ<53..48> - @m72_lib.M72	102C3
MEM_A_DQ<49>	MEM_A_DQ<49> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<50>	MEM_A_DQ<50> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<51>	MEM_A_DQ<51> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<52>	MEM_A_DQ<52> - @m72_lib.M72	17B8 31A3
MEM_A_DQ<53>	MEM_A_DQ<53> - @m72_lib.M72	17B8 31A3
MEM_A_DQ<54>	MEM_A_DQ<54> - @m72_lib.M72	7B7 17B8 31A3 102C3

MEM_A_DQ<55>	MEM_A_DQ<55> - @m72_lib.M72	17B8 31A3 102C3
MEM_A_DQ<56>	MEM_A_DQ<56> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<58..56>	MEM_A_DQ<58..56> - @m72_lib.M72	102C3
MEM_A_DQ<57>	MEM_A_DQ<57> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<58>	MEM_A_DQ<58> - @m72_lib.M72	17B8 31A6
MEM_A_DQ<59>	MEM_A_DQ<59> - @m72_lib.M72	7B7 17B8 31A6 102C3
MEM_A_DQ<60>	MEM_A_DQ<60> - @m72_lib.M72	17A8 31A3
MEM_A_DQ<63..60>	MEM_A_DQ<63..60> - @m72_lib.M72	102C3
MEM_A_DQ<61>	MEM_A_DQ<61> - @m72_lib.M72	17A8 31A3
MEM_A_DQ<62>	MEM_A_DQ<62> - @m72_lib.M72	17A8 31A3
MEM_A_DQ<63>	MEM_A_DQ<63> - @m72_lib.M72	17A8 31A3
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @m72_lib.M72	7B7 17C5 31D6 102B3
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @m72_lib.M72	7B7 17C5 31D6 102B3
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @m72_lib.M72	7B7 17C5 31C6 102B3
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @m72_lib.M72	7B7 17C5 31C3 102B3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @m72_lib.M72	7B7 17C5 31B6 102B3
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @m72_lib.M72	7B7 17C5 31B3 102B3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @m72_lib.M72	7B7 17C5 31A6 102B3
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @m72_lib.M72	7B7 17C5 31A3 102B3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @m72_lib.M72	7B7 17C5 31D6 102B3
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @m72_lib.M72	7B7 17C5 31D6 102B3
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @m72_lib.M72	7B7 17C5 31C6 102B3
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @m72_lib.M72	7B7 17C5 31C3 102B3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @m72_lib.M72	7B7 17C5 31B6 102B3
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @m72_lib.M72	7B7 17C5 31B3 102B3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @m72_lib.M72	7B7 17C5 31A6 102B3
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @m72_lib.M72	7B7 17C5 31A3 102B3
MEM_A_RAS_L	MEM_A_RAS_L - @m72_lib.M72	17B5 31B3 33B6 102D3
MEM_A_SA<0>	MEM_A_SA<0> - @m72_lib.M72	31A4
MEM_A_SA<1>	MEM_A_SA<1> - @m72_lib.M72	31A4
MEM_A_WE_L	MEM_A_WE_L - @m72_lib.M72	17B5 31B6 33B6 102D3
MEM_B_A<0>	MEM_B_A<0> - @m72_lib.M72	17C1 32B3 33B6
MEM_B_A<14..0>	MEM_B_A<14..0> - @m72_lib.M72	102D1
MEM_B_A<1>	MEM_B_A<1> - @m72_lib.M72	17C1 32B6 33B6
MEM_B_A<2>	MEM_B_A<2> - @m72_lib.M72	17B1 32B3 33B6
MEM_B_A<3>	MEM_B_A<3> - @m72_lib.M72	17B1 32B6 33B6
MEM_B_A<4>	MEM_B_A<4> - @m72_lib.M72	17B1 32C3 33B6
MEM_B_A<5>	MEM_B_A<5> - @m72_lib.M72	17B1 32C6 33B6
MEM_B_A<6>	MEM_B_A<6> - @m72_lib.M72	17B1 32C3 33B6
MEM_B_A<7>	MEM_B_A<7> - @m72_lib.M72	17B1 32C3 33B6
MEM_B_A<8>	MEM_B_A<8> - @m72_lib.M72	17B1 32C6 33B6
MEM_B_A<9>	MEM_B_A<9> - @m72_lib.M72	17B1 32C6 33B6
MEM_B_A<10>	MEM_B_A<10> - @m72_lib.M72	17B1 32B6 33B6
MEM_B_A<11>	MEM_B_A<11> - @m72_lib.M72	17B1 32C3 33A6
MEM_B_A<12>	MEM_B_A<12> - @m72_lib.M72	17B1 32C6 33A6
MEM_B_A<13>	MEM_B_A<13> - @m72_lib.M72	17B1 32B3 33A6
MEM_B_A<14>	MEM_B_A<14> - @m72_lib.M72	16C6 32C3 33A6
MEM_B_BS<0>	MEM_B_BS<0> - @m72_lib.M72	17D1 32B6 33A6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m72_lib.M72	102D1
MEM_B_BS<1>	MEM_B_BS<1> - @m72_lib.M72	17D1 32B3 33A6
MEM_B_BS<2>	MEM_B_BS<2> - @m72_lib.M72	17D1 32C6 33A6
MEM_B_CAS_L	MEM_B_CAS_L - @m72_lib.M72	17D1 32B6 33A6 102D1
MEM_B_DM<0>	MEM_B_DM<0> - @m72_lib.M72	17D1 32D3 102C1
MEM_B_DM<1>	MEM_B_DM<1> - @m72_lib.M72	17D1 32D3 102C1
MEM_B_DM<2>	MEM_B_DM<2> - @m72_lib.M72	17C1 32C3 102C1
MEM_B_DM<3>	MEM_B_DM<3> - @m72_lib.M72	17C1 32C6 102C1
MEM_B_DM<4>	MEM_B_DM<4> - @m72_lib.M72	17C1 32B3 102C1
MEM_B_DM<5>	MEM_B_DM<5> - @m72_lib.M72	17C1 32B6 102C1
MEM_B_DM<6>	MEM_B_DM<6> - @m72_lib.M72	17C1 32A3 102C1
MEM_B_DM<7>	MEM_B_DM<7> - @m72_lib.M72	17C1 32A6 102C1
MEM_B_DQ<0>	MEM_B_DQ<0> - @m72_lib.M72	17D4 32D6
MEM_B_DQ<5..0>	MEM_B_DQ<5..0> - @m72_lib.M72	102D1
MEM_B_DQ<1>	MEM_B_DQ<1> - @m72_lib.M72	17D4 32D6
MEM_B_DQ<2>	MEM_B_DQ<2> - @m72_lib.M72	17D4 32D6
MEM_B_DQ<3>	MEM_B_DQ<3> - @m72_lib.M72	17D4 32D6
MEM_B_DQ<4>	MEM_B_DQ<4> - @m72_lib.M72	17D4 32D3
MEM_B_DQ<5>	MEM_B_DQ<5> - @m72_lib.M72	17D4 32D3
MEM_B_DQ<6>	MEM_B_DQ<6> - @m72_lib.M72	7B7 17D4 32D3 102D1
MEM_B_DQ<7>	MEM_B_DQ<7> - @m72_lib.M72	17D4 32D3 102D1
MEM_B_DQ<8>	MEM_B_DQ<8> - @m72_lib.M72	7B7 17C4 32D6 102D1
MEM_B_DQ<9>	MEM_B_DQ<9> - @m72_lib.M72	17C4 32D6
MEM_B_DQ<15..9>	MEM_B_DQ<15..9> - @m72_lib.M72	102D1
MEM_B_DQ<10>	MEM_B_DQ<10> - @m72_lib.M72	17C4 32D6
MEM_B_DQ<11>	MEM_B_DQ<11> - @m72_lib.M72	17C4 32D6
MEM_B_DQ<12>	MEM_B_DQ<12> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<13>	MEM_B_DQ<13> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<14>	MEM_B_DQ<14> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<15>	MEM_B_DQ<15> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<16>	MEM_B_DQ<16> - @m72_lib.M72	17C4 32D6
MEM_B_DQ<22..16>	MEM_B_DQ<22..16> - @m72_lib.M72	102D1
MEM_B_DQ<17>	MEM_B_DQ<17> - @m72_lib.M72	17C4 32D6
MEM_B_DQ<18>	MEM_B_DQ<18> - @m72_lib.M72	17C4 32C6
MEM_B_DQ<19>	MEM_B_DQ<19> - @m72_lib.M72	17C4 32C6
MEM_B_DQ<20>	MEM_B_DQ<20> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<21>	MEM_B_DQ<21> - @m72_lib.M72	17C4 32D3
MEM_B_DQ<22>	MEM_B_DQ<22> - @m72_lib.M72	17C4 32C3
MEM_B_DQ<23>	MEM_B_DQ<23> - @m72_lib.M72	7B7 17C4 32C3 102D1
MEM_B_DQ<24>	MEM_B_DQ<24> - @m72_lib.M72	17C4 32C6 102C1
MEM_B_DQ<25>	MEM_B_DQ<25> - @m72_lib.M72	7B7 17C4 32C6 102C1
MEM_B_DQ<26>	MEM_B_DQ<26> - @m72_lib.M72	17C4 32C6
MEM_B_DQ<31..26>	MEM_B_DQ<31..26> - @m72_lib.M72	102C1
MEM_B_DQ<27>	MEM_B_DQ<27> - @m72_lib.M72	17C4 32C6
MEM_B_DQ<28>	MEM_B_DQ<28> - @m72_lib.M72	17C4 32C3
MEM_B_DQ<29>	MEM_B_DQ<29> - @m72_lib.M72	17C4 32C3
MEM_B_DQ<30>	MEM_B_DQ<30> - @m72_lib.M72	17C4 32C3
MEM_B_DQ<31>	MEM_B_DQ<31> - @m72_lib.M72	17C4 32C3
MEM_B_DQ<32>	MEM_B_DQ<32> - @m72_lib.M72	17C4 32B6
MEM_B_DQ<37..32>	MEM_B_DQ<37..32> - @m72_lib.M72	102C1
MEM_B_DQ<33>	MEM_B_DQ<33> - @m72_lib.M72	17C4 32B6
MEM_B_DQ<34>	MEM_B_DQ<34> - @m72_lib.M72	17B4 32B6
MEM_B_DQ<35>	MEM_B_DQ<35> - @m72_lib.M72	17B4 32B6
MEM_B_DQ<36>	MEM_B_DQ<36> - @m72_lib.M72	17B4 32B3
MEM_B_DQ<37>	MEM_B_DQ<37> - @m72_lib.M72	17B4 32B3
MEM_B_DQ<38>	MEM_B_DQ<38> - @m72_lib.M72	7A7 17B4 32B3 102C1
MEM_B_DQ<39>	MEM_B_DQ<39> - @m72_lib.M72	17B4 32B3 102C1
MEM_B_DQ<40>	MEM_B_DQ<40> - @m72_lib.M72	17B4 32B6
MEM_B_DQ<43..40>	MEM_B_DQ<43..40> - @m72_lib.M72	102C1
MEM_B_DQ<41>	MEM_B_DQ<41> - @m72_lib.M72	17B4 32B6
MEM_B_DQ<42>	MEM_B_DQ<42> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<43>	MEM_B_DQ<43> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<44>	MEM_B_DQ<44> - @m72_lib.M72	7A7 17B4 32B3 102C1
MEM_B_DQ<45>	MEM_B_DQ<45> - @m72_lib.M72	17B4 32B3
MEM_B_DQ<47..45>	MEM_B_DQ<47..45> - @m72_lib.M72	102C1
MEM_B_DQ<46>	MEM_B_DQ<46> - @m72_lib.M72	17B4 32A3
MEM_B_DQ<47>	MEM_B_DQ<47> - @m72_lib.M72	17B4 32A3
MEM_B_DQ<48>	MEM_B_DQ<48> - @m72_lib.M72	7A7 17B4 32A6 102C1
MEM_B_DQ<49>	MEM_B_DQ<49> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<55..49>	MEM_B_DQ<55..49> - @m72_lib.M72	102C1
MEM_B_DQ<50>	MEM_B_DQ<50> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<51>	MEM_B_DQ<51> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<52>	MEM_B_DQ<52> - @m72_lib.M72	17B4 32A3
MEM_B_DQ<53>	MEM_B_DQ<53> - @m72_lib.M72	17B4 32A3
MEM_B_DQ<54>	MEM_B_DQ<54> - @m72_lib.M72	17B4 32A3
MEM_B_DQ<55>	MEM_B_DQ<55> - @m72_lib.M72	17B4 32A3

MEM_B_DQ<56>	MEM_B_DQ<56> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<61..56>	MEM_B_DQ<61..56> - @m72_lib.M72	102C1
MEM_B_DQ<57>	MEM_B_DQ<57> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<58>	MEM_B_DQ<58> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<59>	MEM_B_DQ<59> - @m72_lib.M72	17B4 32A6
MEM_B_DQ<60>	MEM_B_DQ<60> - @m72_lib.M72	17A4 32A3
MEM_B_DQ<61>	MEM_B_DQ<61> - @m72_lib.M72	17A4 32A3
MEM_B_DQ<62>	MEM_B_DQ<62> - @m72_lib.M72	7A7 17A4 32A3 102C1
MEM_B_DQ<63>	MEM_B_DQ<63> - @m72_lib.M72	17A4 32A3 102C1
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @m72_lib.M72	7A7 17C1 32D6 102B1
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @m72_lib.M72	7A7 17C1 32D6 102B1
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @m72_lib.M72	7A7 17C1 32C6 102B1
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @m72_lib.M72	7A7 17C1 32C3 102B1
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @m72_lib.M72	7A7 17C1 32B6 102B1
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @m72_lib.M72	7A7 17C1 32B3 102B1
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @m72_lib.M72	7A7 17C1 32A6 102B1
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @m72_lib.M72	7A7 17C1 32A3 102B1
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @m72_lib.M72	7A7 17C1 32D6 102B1
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @m72_lib.M72	7A7 17C1 32D6 102B1
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @m72_lib.M72	7A7 17C1 32C6 102B1
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @m72_lib.M72	7A7 17C1 32C3 102B1
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @m72_lib.M72	7A7 17C1 32B6 102B1
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @m72_lib.M72	7A7 17C1 32B3 102B1
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @m72_lib.M72	7A7 17C1 32A6 102B1
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @m72_lib.M72	7A7 17C1 32A3 102B1
MEM_B_RAS_L	MEM_B_RAS_L - @m72_lib.M72	17B1 32B3 33A6 102D1
MEM_B_SA<0>	MEM_B_SA<0> - @m72_lib.M72	32A4
MEM_B_SA<1>	MEM_B_SA<1> - @m72_lib.M72	32A4
MEM_B_WE_L	MEM_B_WE_L - @m72_lib.M72	17B1 32B6 33A6 102D1
MEM_CKE<0>	MEM_CKE<0> - @m72_lib.M72	16D3 31C6 33D6
MEM_CKE<1..0>	MEM_CKE<1..0> - @m72_lib.M72	102D3
MEM_CKE<1>	MEM_CKE<1> - @m72_lib.M72	16D3 31C3 33D6
MEM_CKE<3>	MEM_CKE<3> - @m72_lib.M72	16D3 32C6 33D6
MEM_CKE<4..3>	MEM_CKE<4..3> - @m72_lib.M72	102D1
MEM_CKE<4>	MEM_CKE<4> - @m72_lib.M72	16D3 32C3 33D6
MEM_CLK_N<0>	MEM_CLK_N<0> - @m72_lib.M72	16D3 31D3
MEM_CLK_N<1..0>	MEM_CLK_N<1..0> - @m72_lib.M72	102D3
MEM_CLK_N<1>	MEM_CLK_N<1> - @m72_lib.M72	16D3 31A3
MEM_CLK_N<3>	MEM_CLK_N<3> - @m72_lib.M72	16D3 32D3
MEM_CLK_N<4..3>	MEM_CLK_N<4..3> - @m72_lib.M72	102D1
MEM_CLK_N<4>	MEM_CLK_N<4> - @m72_lib.M72	16D3 32A3
MEM_CLK_P<0>	MEM_CLK_P<0> - @m72_lib.M72	16D3 31D3
MEM_CLK_P<1..0>	MEM_CLK_P<1..0> - @m72_lib.M72	102D3
MEM_CLK_P<1>	MEM_CLK_P<1> - @m72_lib.M72	16D3 31A3
MEM_CLK_P<3>	MEM_CLK_P<3> - @m72_lib.M72	16D3 32D3
MEM_CLK_P<4..3>	MEM_CLK_P<4..3> - @m72_lib.M72	102D1
MEM_CLK_P<4>	MEM_CLK_P<4> - @m72_lib.M72	16D3 32A3
MEM_CS_L<0>	MEM_CS_L<0> - @m72_lib.M72	16D3 31B3 33D6
MEM_CS_L<1..0>	MEM_CS_L<1..0> - @m72_lib.M72	102D3
MEM_CS_L<1>	MEM_CS_L<1> - @m72_lib.M72	16D3 31B6 33D6
MEM_CS_L<2>	MEM_CS_L<2> - @m72_lib.M72	16D3 32B3 33D6
MEM_CS_L<3..2>	MEM_CS_L<3..2> - @m72_lib.M72	102D1
MEM_CS_L<3>	MEM_CS_L<3> - @m72_lib.M72	16C3 32B6 33D6
MEM_ODT<0>	MEM_ODT<0> - @m72_lib.M72	16C3 31B3 33C6
MEM_ODT<1..0>	MEM_ODT<1..0> - @m72_lib.M72	102D3
MEM_ODT<1>	MEM_ODT<1> - @m72_lib.M72	16C3 31B6 33C6
MEM_ODT<2>	MEM_ODT<2> - @m72_lib.M72	16C3 32B3 33C6
MEM_ODT<3..2>	MEM_ODT<3..2> - @m72_lib.M72	102D1
MEM_ODT<3>	MEM_ODT<3> - @m72_lib.M72	16C3 32B6 33C6
MEM_RCOMP	MEM_RCOMP - @m72_lib.M72	16C4
MEM_RCOMP_L	MEM_RCOMP_L - @m72_lib.M72	16C4
MEM_RCOMP_VOH	MEM_RCOMP_VOH - @m72_lib.M72	16C4
MEM_RCOMP_VOL	MEM_RCOMP_VOL - @m72_lib.M72	16C4
MINI_RESET_L	MINI_RESET_L - @m72_lib.M72	28D1 34C3
MXM_DETECT_L	MXM_DETECT_L - @m72_lib.M72	85C4
MXM_PIN170	MXM_PIN170 - @m72_lib.M72	85B5
MXM_PWRSRC_SENSE	MXM_PWRSRC_SENSE - @m72_lib.M72	53C3
MXM_ROM_WP	MXM_ROM_WP - @m72_lib.M72	85C3
MXM_SENSE_I_R	MXM_SENSE_I_R - @m72_lib.M72	53C3
NB_BSEL<0>	NB_BSEL<0> - @m72_lib.M72	13C6 16C6 30C8 100B3
NB_BSEL<1>	NB_BSEL<1> - @m72_lib.M72	13C6 16C6 30B8 100B3
NB_BSEL<2>	NB_BSEL<2> - @m72_lib.M72	13C3 16B6 30B8 100A3
NB_CFG<3>	NB_CFG<3> - @m72_lib.M72	7B3 13C3 16B6
NB_CFG<4>	NB_CFG<4> - @m72_lib.M72	7B3 13C6 16B6
NB_CFG<5>	NB_CFG<5> - @m72_lib.M72	7B3 13C6 16B6 16D7
NB_CFG<6>	NB_CFG<6> - @m72_lib.M72	7B3 13C6 16B6
NB_CFG<7>	NB_CFG<7> - @m72_lib.M72	7B3 13C6 16B6
NB_CFG<8>	NB_CFG<8> - @m72_lib.M72	13C3 16B6
NB_CFG<9>	NB_CFG<9> - @m72_lib.M72	16B6 16D7
NB_CFG<16>	NB_CFG<16> - @m72_lib.M72	16B6 16D7
NB_CFG<19>	NB_CFG<19> - @m72_lib.M72	7C3 16B6 16C7
NB_CFG<20>	NB_CFG<20> - @m72_lib.M72	16B6 16C7
NB_CLINK_VREF	NB_CLINK_VREF - @m72_lib.M72	16A4 104B3
NB_CLKREQ_L	NB_CLKREQ_L - @m72_lib.M72	16A3 29B3 30C2
NB_FSB_RCOMP	NB_FSB_RCOMP - @m72_lib.M72	14A5
NB_FSB_SCOMP	NB_FSB_SCOMP - @m72_lib.M72	14A5
NB_FSB_SCOMP_L	NB_FSB_SCOMP_L - @m72_lib.M72	14A5
NB_FSB_SWING	NB_FSB_SWING - @m72_lib.M72	14A5
NB_FSB_VREF	NB_FSB_VREF - @m72_lib.M72	14A5
NB_RESET_L	NB_RESET_L - @m72_lib.M72	7C7 16B6 28D1
NB_SB_SYNC_L	NB_SB_SYNC_L - @m72_lib.M72	16A3 25B5
NB_TEST1	NB_TEST1 - @m72_lib.M72	16A4
NB_TEST2	NB_TEST2 - @m72_lib.M72	16A4
NB_VCCSM_LF1	NB_VCCSM_LF1 - @m72_lib.M72	18A6
NB_VCCSM_LF2	NB_VCCSM_LF2 - @m72_lib.M72	18A6
NB_VCCSM_LF3	NB_VCCSM_LF3 - @m72_lib.M72	18A6
NB_VCCSM_LF4	NB_VCCSM_LF4 - @m72_lib.M72	18A6
NB_VCCSM_LF5	NB_VCCSM_LF5 - @m72_lib.M72	18A6
NB_VCCSM_LF6	NB_VCCSM_LF6 - @m72_lib.M72	18A6
NB_VCCSM_LF7	NB_VCCSM_LF7 - @m72_lib.M72	18A6
NB_VTTLF_CAP1	NB_VTTLF_CAP1 - @m72_lib.M72	19A4
NB_VTTLF_CAP2	NB_VTTLF_CAP2 - @m72_lib.M72	19A4
NB_VTTLF_CAP3	NB_VTTLF_CAP3 - @m72_lib.M72	19A4
NC_SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN - @m72_lib.M72	50D3
	SMC_BATT_CHG_EN - @m72_lib.M72	49C8 50D5
NC_SMC_BATT_ISET	NC_SMC_BATT_ISET - @m72_lib.M72	50D3
	SMC_BATT_ISET - @m72_lib.M72	49B5 50D5
NC_SMC_BATT_TRICKLE_ EN_L	NC_SMC_BATT_TRICKLE_EN_L - @m72_lib.M72	50D3
	SMC_BATT_TRICKLE_EN_L - @m72_lib.M72	49C8 50D5
NC_SMC_BATT_VSET	NC_SMC_BATT_VSET - @m72_lib.M72	50D3
	SMC_BATT_VSET - @m72_lib.M72	49B5 50D5
NC_SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE - @m72_lib.M72	50B3
	SMC_NB_1V8_ISENSE - @m72_lib.M72	49A8 50B5
NC_SMC_NB_CORE_ISENS E	NC_SMC_NB_CORE_ISENSE - @m72_lib.M72	50B3
	SMC_NB_CORE_ISENSE - @m72_lib.M72	49A8 50B5
NC_SMC_SYS_ISET	NC_SMC_SYS_ISET - @m72_lib.M72	50D3
	SMC_SYS_ISET - @m72_lib.M72	49B5 50D5
NC_SMC_SYS_VSET	NC_SMC_SYS_VSET - @m72_lib.M72	50D3
	SMC_SYS_VSET - @m72_lib.M72	49B5 50D5
ODD_PWR_EN_L	ODD_PWR_EN_L - @m72_lib.M72	24A4 24A6
ODD_RST_5VTOL_L	ODD_RST_5VTOL_L - @m72_lib.M72	7B3 24B6 44C6 103D3

ODD_THRMD_N	ODD_THRMD_N - @m72_lib.M72	55A5 55B6 108A3
ODD_THRMD_P	ODD_THRMD_P - @m72_lib.M72	55B5 55B6 108A3
P1V8S0_EN_L	P1V8S0_EN_L - @m72_lib.M72	78A7
P1V8S0_EN_L_RC	P1V8S0_EN_L_RC - @m72_lib.M72	78A6
P1V8S0_GDRV	P1V8S0_GDRV - @m72_lib.M72	78B7
P1V8S0_SS	P1V8S0_SS - @m72_lib.M72	78B6
P1V8S0_SS_RC	P1V8S0_SS_RC - @m72_lib.M72	78B7
P2V5S0_EN	P2V5S0_EN - @m72_lib.M72	77B5
P2V5S0_SW	P2V5S0_SW - @m72_lib.M72	77B4 108D1
P2V5S0_VFB	P2V5S0_VFB - @m72_lib.M72	77B4
P3V3S0_EN_L	P3V3S0_EN_L - @m72_lib.M72	78C5
P3V3S0_SS	P3V3S0_SS - @m72_lib.M72	78C4
P3V3S5_FB	P3V3S5_FB - @m72_lib.M72	77D5
P3V3S5_SW	P3V3S5_SW - @m72_lib.M72	77D5 108D1
P5VREG_FCB	P5VREG_FCB - @m72_lib.M72	76A3 76B5
P5VREG_FSEL	P5VREG_FSEL - @m72_lib.M72	76A2 76B4
P5VS0_EN_L	P5VS0_EN_L - @m72_lib.M72	78D5
P5VS0_SS	P5VS0_SS - @m72_lib.M72	78D4
P5VS3_EN_L	P5VS3_EN_L - @m72_lib.M72	78D8
P5VS3_SS	P5VS3_SS - @m72_lib.M72	78D7
P5VS5_EN	P5VS5_EN - @m72_lib.M72	77D6
P12V_S3_DRAIN	P12V_S3_DRAIN - @m72_lib.M72	78C1
P12V_S3_EN_L	P12V_S3_EN_L - @m72_lib.M72	78D3
PANEL_ID	PANEL_ID - @m72_lib.M72	28B2
	TP_SB_GPIO20 - @m72_lib.M72	25C5 28B1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @m72_lib.M72	37C4 108C3
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @m72_lib.M72	37C4 108C3
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @m72_lib.M72	7B8 24C5 37C8 104C3
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @m72_lib.M72	7B8 24C5 37C8 104C3
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @m72_lib.M72	24C5 37C8 104C3
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @m72_lib.M72	24C5 37C8 104C3
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @m72_lib.M72	7D6 37C4 108C3
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @m72_lib.M72	7D6 37C4 108C3
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @m72_lib.M72	40C3 108C3
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @m72_lib.M72	40C3 108C3
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @m72_lib.M72	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_N - @m72_lib.M72	24D5 42A1
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @m72_lib.M72	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_P - @m72_lib.M72	24D5 42A1
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @m72_lib.M72	40C1 42A1 104C3
	TP_PCIE_FW_R2D_C_N - @m72_lib.M72	24D5 42A3
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @m72_lib.M72	40C1 42A1 104C3
	TP_PCIE_FW_R2D_C_P - @m72_lib.M72	24D5 42A3
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @m72_lib.M72	7D6 40C3 108C3
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @m72_lib.M72	7D6 40C3 108C3
PCIE_MINI_D2R_N	PCIE_MINI_D2R_N - @m72_lib.M72	7B8 24D5 34C8 104C3
PCIE_MINI_D2R_P	PCIE_MINI_D2R_P - @m72_lib.M72	7B8 24C5 34C8 104C3
PCIE_MINI_R2D_C_N	PCIE_MINI_R2D_C_N - @m72_lib.M72	24C5 34B8 104C3
PCIE_MINI_R2D_C_P	PCIE_MINI_R2D_C_P - @m72_lib.M72	24C5 34B8 104C3
PCIE_MINI_R2D_N	PCIE_MINI_R2D_N - @m72_lib.M72	34B6 108C3
PCIE_MINI_R2D_P	PCIE_MINI_R2D_P - @m72_lib.M72	34B6 108B3
PCIE_WAKE_L	PCIE_WAKE_L - @m72_lib.M72	25C8 34C6 37B8
PCI_AD<0>	PCI_AD<0> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_0 - @m72_lib.M72	28C4
PCI_AD<18..0>	PCI_AD<18..0> - @m72_lib.M72	104D3
	TP_PCI_AD_18 - @m72_lib.M72	28B4
PCI_AD<1>	PCI_AD<1> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_1 - @m72_lib.M72	28C4
PCI_AD<2>	PCI_AD<2> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_2 - @m72_lib.M72	28C4
PCI_AD<3>	PCI_AD<3> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_3 - @m72_lib.M72	28C4
PCI_AD<4>	PCI_AD<4> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_4 - @m72_lib.M72	7D2 28C4
PCI_AD<5>	PCI_AD<5> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_5 - @m72_lib.M72	28C4
PCI_AD<6>	PCI_AD<6> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_6 - @m72_lib.M72	28C4
PCI_AD<7>	PCI_AD<7> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_7 - @m72_lib.M72	28C4
PCI_AD<8>	PCI_AD<8> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_8 - @m72_lib.M72	28C4
PCI_AD<9>	PCI_AD<9> - @m72_lib.M72	24B8 28C5
	TP_PCI_AD_9 - @m72_lib.M72	28C4
PCI_AD<10>	PCI_AD<10> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_10 - @m72_lib.M72	28C4
PCI_AD<11>	PCI_AD<11> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_11 - @m72_lib.M72	28C4
PCI_AD<12>	PCI_AD<12> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_12 - @m72_lib.M72	28C4
PCI_AD<13>	PCI_AD<13> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_13 - @m72_lib.M72	28C4
PCI_AD<14>	PCI_AD<14> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_14 - @m72_lib.M72	28C4
PCI_AD<15>	PCI_AD<15> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_15 - @m72_lib.M72	28C4
PCI_AD<16>	PCI_AD<16> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_16 - @m72_lib.M72	28C4
PCI_AD<17>	PCI_AD<17> - @m72_lib.M72	24A8 28C5
	TP_PCI_AD_17 - @m72_lib.M72	28C4
PCI_AD<18>	PCI_AD<18> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_18 - @m72_lib.M72	28B4
PCI_AD<19>	PCI_AD<19> - @m72_lib.M72	24A8 28B5 104D3
	TP_PCI_AD_19 - @m72_lib.M72	28B4
PCI_AD<20>	PCI_AD<20> - @m72_lib.M72	24A8 28B5 104D3
	TP_PCI_AD_20 - @m72_lib.M72	28B4
PCI_AD<21>	PCI_AD<21> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_21 - @m72_lib.M72	28B4
PCI_AD<31..21>	PCI_AD<31..21> - @m72_lib.M72	104D3
	TP_PCI_AD_31 - @m72_lib.M72	28B4
PCI_AD<22>	PCI_AD<22> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_22 - @m72_lib.M72	28B4
PCI_AD<23>	PCI_AD<23> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_23 - @m72_lib.M72	28B4
PCI_AD<24>	PCI_AD<24> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_24 - @m72_lib.M72	28B4
PCI_AD<25>	PCI_AD<25> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_25 - @m72_lib.M72	28B4
PCI_AD<26>	PCI_AD<26> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_26 - @m72_lib.M72	28B4
PCI_AD<27>	PCI_AD<27> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_27 - @m72_lib.M72	28B4
PCI_AD<28>	PCI_AD<28> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_28 - @m72_lib.M72	28B4
PCI_AD<29>	PCI_AD<29> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_29 - @m72_lib.M72	28B4
PCI_AD<30>	PCI_AD<30> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_30 - @m72_lib.M72	28B4
PCI_AD<31>	PCI_AD<31> - @m72_lib.M72	24A8 28B5
	TP_PCI_AD_31 - @m72_lib.M72	28B4
PCI_CLK33M_LPCPLUS	PCI_CLK33M_LPCPLUS - @m72_lib.M72	7D4 30A3 51C4 105C3
PCI_CLK33M_SB	PCI_CLK33M_SB - @m72_lib.M72	7B8 24A6 30A3 105B3
PCI_CLK33M_SMC	PCI_CLK33M_SMC - @m72_lib.M72	7C6 30A3 49C8 105B3
PCI_CLK33M_TPM	PCI_CLK33M_TPM - @m72_lib.M72	105B3

PCI_C_BE_L<0>	PCI_C_BE_L<0> - @m72_lib.M72	24B6 28B5
	TP_PCI_C_BE_L_0 - @m72_lib.M72	28B4
PCI_C_BE_L<3..0>	PCI_C_BE_L<3..0> - @m72_lib.M72	104D3
	TP_PCI_C_BE_L_3 - @m72_lib.M72	28B4
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @m72_lib.M72	24A6 28B5
	TP_PCI_C_BE_L_1 - @m72_lib.M72	28B4
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @m72_lib.M72	24A6 28B5
	TP_PCI_C_BE_L_2 - @m72_lib.M72	28B4
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @m72_lib.M72	24A6 28B5
	TP_PCI_C_BE_L_3 - @m72_lib.M72	28B4
PCI_DEVSEL_L	PCI_DEVSEL_L - @m72_lib.M72	24A4 24A6 104D3
PCI_FRAME_L	PCI_FRAME_L - @m72_lib.M72	24A4 24A6 104D3
PCI_FW_GNT_L	PCI_FW_GNT_L - @m72_lib.M72	24B5 104D3
	BOOT_LPC_SPI_L - @m72_lib.M72	7D4 24B5 51B6
PCI_FW_REQ_L	PCI_FW_REQ_L - @m72_lib.M72	24A4 24B6 104D3
PCI_GNT1_L	PCI_GNT1_L - @m72_lib.M72	104D3
PCI_GNT2_L	PCI_GNT2_L - @m72_lib.M72	104C3
PCI_IRDY_L	PCI_IRDY_L - @m72_lib.M72	24A4 24A6 104D3
PCI_LOCK_L	PCI_LOCK_L - @m72_lib.M72	24A4 24A6 104D3
PCI_PAR	PCI_PAR - @m72_lib.M72	24A6 28B5 104D3
	TP_PCI_PAR - @m72_lib.M72	28B4
PCI_PERR_L	PCI_PERR_L - @m72_lib.M72	24A4 24A6 104D3
PCI_PME_FW_L	PCI_PME_FW_L - @m72_lib.M72	25B5 25C5 40C3
PCI_REQ1_L	PCI_REQ1_L - @m72_lib.M72	7C3 24A4 24B6 104D3
PCI_REQ2_L	PCI_REQ2_L - @m72_lib.M72	7C3 24A4 24B6 104D3
PCI_RST_L	PCI_RST_L - @m72_lib.M72	24A6 28B5
	TP_PCI_RST_L - @m72_lib.M72	28B4
PCI_SERR_L	PCI_SERR_L - @m72_lib.M72	7D2 24A4 24A6 28C4 104D3
PCI_STOP_L	PCI_STOP_L - @m72_lib.M72	24A4 24A6 104D3
PCI_TRDY_L	PCI_TRDY_L - @m72_lib.M72	24A4 24A6 104D3
PEG_COMP	PEG_COMP - @m72_lib.M72	15D3
PEG_D2R_N<0>	PEG_D2R_N<0> - @m72_lib.M72	15D3 84C4
PEG_D2R_N<6..0>	PEG_D2R_N<6..0> - @m72_lib.M72	101D3
PEG_D2R_N<1>	PEG_D2R_N<1> - @m72_lib.M72	15D3 84C4
PEG_D2R_N<2>	PEG_D2R_N<2> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<3>	PEG_D2R_N<3> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<4>	PEG_D2R_N<4> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<5>	PEG_D2R_N<5> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<6>	PEG_D2R_N<6> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<7>	PEG_D2R_N<7> - @m72_lib.M72	7A7 15D3 84B4 101D3
PEG_D2R_N<8>	PEG_D2R_N<8> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<15..8>	PEG_D2R_N<15..8> - @m72_lib.M72	101D3
PEG_D2R_N<9>	PEG_D2R_N<9> - @m72_lib.M72	15D3 84B4
PEG_D2R_N<10>	PEG_D2R_N<10> - @m72_lib.M72	15C3 84B4
PEG_D2R_N<11>	PEG_D2R_N<11> - @m72_lib.M72	15C3 84A4
PEG_D2R_N<12>	PEG_D2R_N<12> - @m72_lib.M72	15C3 84A4
PEG_D2R_N<13>	PEG_D2R_N<13> - @m72_lib.M72	15C3 84A4
PEG_D2R_N<14>	PEG_D2R_N<14> - @m72_lib.M72	15C3 84A4
PEG_D2R_N<15>	PEG_D2R_N<15> - @m72_lib.M72	15C3 84A4
PEG_D2R_P<0>	PEG_D2R_P<0> - @m72_lib.M72	15C3 84C4
PEG_D2R_P<6..0>	PEG_D2R_P<6..0> - @m72_lib.M72	101D3
PEG_D2R_P<1>	PEG_D2R_P<1> - @m72_lib.M72	15C3 84C4
PEG_D2R_P<2>	PEG_D2R_P<2> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<3>	PEG_D2R_P<3> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<4>	PEG_D2R_P<4> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<5>	PEG_D2R_P<5> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<6>	PEG_D2R_P<6> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<7>	PEG_D2R_P<7> - @m72_lib.M72	7A7 15C3 84B4 101D3
PEG_D2R_P<8>	PEG_D2R_P<8> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<15..8>	PEG_D2R_P<15..8> - @m72_lib.M72	101D3
PEG_D2R_P<9>	PEG_D2R_P<9> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<10>	PEG_D2R_P<10> - @m72_lib.M72	15C3 84B4
PEG_D2R_P<11>	PEG_D2R_P<11> - @m72_lib.M72	15C3 84A4
PEG_D2R_P<12>	PEG_D2R_P<12> - @m72_lib.M72	15C3 84A4
PEG_D2R_P<13>	PEG_D2R_P<13> - @m72_lib.M72	15C3 84A4
PEG_D2R_P<14>	PEG_D2R_P<14> - @m72_lib.M72	15C3 84A4
PEG_D2R_P<15>	PEG_D2R_P<15> - @m72_lib.M72	15C3 84A4
PEG_R2D_C_N<0>	PEG_R2D_C_N<0> - @m72_lib.M72	15C3 84C8
PEG_R2D_C_N<15..0>	PEG_R2D_C_N<15..0> - @m72_lib.M72	101D3
PEG_R2D_C_N<1>	PEG_R2D_C_N<1> - @m72_lib.M72	15C3 84C8
PEG_R2D_C_N<2>	PEG_R2D_C_N<2> - @m72_lib.M72	15C3 84B8
PEG_R2D_C_N<3>	PEG_R2D_C_N<3> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<4>	PEG_R2D_C_N<4> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<5>	PEG_R2D_C_N<5> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<6>	PEG_R2D_C_N<6> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<7>	PEG_R2D_C_N<7> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<8>	PEG_R2D_C_N<8> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<9>	PEG_R2D_C_N<9> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_N<10>	PEG_R2D_C_N<10> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_N<11>	PEG_R2D_C_N<11> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_N<12>	PEG_R2D_C_N<12> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_N<13>	PEG_R2D_C_N<13> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_N<14>	PEG_R2D_C_N<14> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_N<15>	PEG_R2D_C_N<15> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_P<0>	PEG_R2D_C_P<0> - @m72_lib.M72	15B3 84C8
PEG_R2D_C_P<15..0>	PEG_R2D_C_P<15..0> - @m72_lib.M72	101D3
PEG_R2D_C_P<1>	PEG_R2D_C_P<1> - @m72_lib.M72	15B3 84C8
PEG_R2D_C_P<2>	PEG_R2D_C_P<2> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<3>	PEG_R2D_C_P<3> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<4>	PEG_R2D_C_P<4> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<5>	PEG_R2D_C_P<5> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<6>	PEG_R2D_C_P<6> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<7>	PEG_R2D_C_P<7> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<8>	PEG_R2D_C_P<8> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<9>	PEG_R2D_C_P<9> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<10>	PEG_R2D_C_P<10> - @m72_lib.M72	15B3 84B8
PEG_R2D_C_P<11>	PEG_R2D_C_P<11> - @m72_lib.M72	15B3 84A8
PEG_R2D_C_P<12>	PEG_R2D_C_P<12> - @m72_lib.M72	15A3 84A8
PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @m72_lib.M72	15A3 84A8
PEG_R2D_C_P<14>	PEG_R2D_C_P<14> - @m72_lib.M72	15A3 84A8
PEG_R2D_C_P<15>	PEG_R2D_C_P<15> - @m72_lib.M72	15A3 84A8
PEG_R2D_N<0>	PEG_R2D_N<0> - @m72_lib.M72	84A7
PEG_R2D_N<15..0>	PEG_R2D_N<15..0> - @m72_lib.M72	101D3
PEG_R2D_N<1>	PEG_R2D_N<1> - @m72_lib.M72	84A7
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PEG_R2D_N<3>	PEG_R2D_N<3> - @m72_lib.M72	84A7
PEG_R2D_N<4>	PEG_R2D_N<4> - @m72_lib.M72	84A7
PEG_R2D_N<5>	PEG_R2D_N<5> - @m72_lib.M72	84A7
PEG_R2D_N<6>	PEG_R2D_N<6> - @m72_lib.M72	84B7
PEG_R2D_N<7>	PEG_R2D_N<7> - @m72_lib.M72	84B7
PEG_R2D_N<8>	PEG_R2D_N<8> - @m72_lib.M72	84B7
PEG_R2D_N<9>	PEG_R2D_N<9> - @m72_lib.M72	84B7
PEG_R2D_N<10>	PEG_R2D_N<10> - @m72_lib.M72	84B7
PEG_R2D_N<11>	PEG_R2D_N<11> - @m72_lib.M72	84B7
PEG_R2D_N<12>	PEG_R2D_N<12> - @m72_lib.M72	84B7
PEG_R2D_N<13>	PEG_R2D_N<13> - @m72_lib.M72	84B7
PEG_R2D_N<14>	PEG_R2D_N<14> - @m72_lib.M72	84C7
PEG_R2D_N<15>	PEG_R2D_N<15> - @m72_lib.M72	84C7
PEG_R2D_P<0>	PEG_R2D_P<0> - @m72_lib.M72	84A7
PEG_R2D_P<15..0>	PEG_R2D_P<15..0> - @m72_lib.M72	101D3
PEG_R2D_P<1>	PEG_R2D_P<1> - @m72_lib.M72	84A7
PEG_R2D_P<2>	PEG_R2D_P<2> - @m72_lib.M72	84A7
PEG_R2D_P<3>	PEG_R2D_P<3> - @m72_lib.M72	84A7
PEG_R2D_P<4>	PEG_R2D_P<4> - @m72_lib.M72	84A7

PEG_R2D_P<5>	PEG_R2D_P<5> - @m72_lib.M72	84B7
PEG_R2D_P<6>	PEG_R2D_P<6> - @m72_lib.M72	84B7
PEG_R2D_P<7>	PEG_R2D_P<7> - @m72_lib.M72	84B7
PEG_R2D_P<8>	PEG_R2D_P<8> - @m72_lib.M72	84B7
PEG_R2D_P<9>	PEG_R2D_P<9> - @m72_lib.M72	84B7
PEG_R2D_P<10>	PEG_R2D_P<10> - @m72_lib.M72	84B7
PEG_R2D_P<11>	PEG_R2D_P<11> - @m72_lib.M72	84B7
PEG_R2D_P<12>	PEG_R2D_P<12> - @m72_lib.M72	84B7
PEG_R2D_P<13>	PEG_R2D_P<13> - @m72_lib.M72	84B7
PEG_R2D_P<14>	PEG_R2D_P<14> - @m72_lib.M72	84C7
PEG_R2D_P<15>	PEG_R2D_P<15> - @m72_lib.M72	84C7
PEG_RESET_L	PEG_RESET_L - @m72_lib.M72	28C1 85C7
PGOOD_0V9_S0	PGOOD_0V9_S0 - @m72_lib.M72	70C4 70C4
PGOOD_1V05_S0	PGOOD_1V05_S0 - @m72_lib.M72	70B4 73B3
PGOOD_1V5_S0	PGOOD_1V5_S0 - @m72_lib.M72	70B4 73B5
PGOOD_1V8_S0	PGOOD_1V8_S0 - @m72_lib.M72	70C4 70D4
PGOOD_1V8_S3	PGOOD_1V8_S3 - @m72_lib.M72	70D4 75C8
PGOOD_1V25_S0	PGOOD_1V25_S0 - @m72_lib.M72	70B4 74B5
PGOOD_2V5_S0	PGOOD_2V5_S0 - @m72_lib.M72	70C4 77B7
PGOOD_3V3_S0	PGOOD_3V3_S0 - @m72_lib.M72	70C8 70D4 77B7
PGOOD_3V3_S3	PGOOD_3V3_S3 - @m72_lib.M72	70D4 76B4
PGOOD_3V3_S5	PGOOD_3V3_S5 - @m72_lib.M72	70B4 77D4
	RSMRST_PWRGD - @m72_lib.M72	49D8 70B2
PGOOD_5V_S0	PGOOD_5V_S0 - @m72_lib.M72	70C4 70C4
PGOOD_5V_S3_L	PGOOD_5V_S3_L - @m72_lib.M72	76A6
PGOOD_12V_S0	PGOOD_12V_S0 - @m72_lib.M72	70B8 76D5
PGOOD_CR_S0	PGOOD_CR_S0 - @m72_lib.M72	70C7
PGOOD_MCH_CORE_S0	PGOOD_MCH_CORE_S0 - @m72_lib.M72	70B4 74B3
PGOOD_S0_OUT1	PGOOD_S0_OUT1 - @m72_lib.M72	70C3
PLT_RST_L	PLT_RST_L - @m72_lib.M72	24A6 28D4
PM_BATLOW_L	PM_BATLOW_L - @m72_lib.M72	25A5 25C3 49B8
PM_BMBUSY_L	PM_BMBUSY_L - @m72_lib.M72	16B6 25D5
PM_CLKRUN_L	PM_CLKRUN_L - @m72_lib.M72	7B8 7D4 25C8 49C5 51B6
PM_DPRSLPVR	PM_DPRSLPVR - @m72_lib.M72	16A6 25C3 71C8 100B3
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @m72_lib.M72	16B7 31C3 49B8
PM_EXTTS_L<1>	PM_EXTTS_L<1> - @m72_lib.M72	16B7 32C3 49B8
PM_LAN_ENABLE	PM_LAN_ENABLE - @m72_lib.M72	25C2 49D8
PM_LATRIGGER_L	PM_LATRIGGER_L - @m72_lib.M72	13C3 24C8
PM_PWRBTN_L	PM_PWRBTN_L - @m72_lib.M72	25C3 49C8
PM_RI_L	PM_RI_L - @m72_lib.M72	25A5 25D5
PM_RSMRST_L	PM_RSMRST_L - @m72_lib.M72	25C2 49C8
PM_S4_STATE_INV	PM_S4_STATE_INV - @m72_lib.M72	78C2
PM_S4_STATE_L	PM_S4_STATE_L - @m72_lib.M72	7C4 7D3 25D3 46C8 49C4
		75D8 78C3 78D8
PM_S4_STATE_L_SMC	PM_S4_STATE_L_SMC - @m72_lib.M72	49C6
PM_SLP_S3_L	PM_SLP_S3_L - @m72_lib.M72	6D8 7C4 25D3 49C4 70A8
		75A5 78A8 78C6 78D6
PM_SLP_S3_L_SMC	PM_SLP_S3_L_SMC - @m72_lib.M72	49C6
PM_SLP_S3_OD	PM_SLP_S3_OD - @m72_lib.M72	6D7
PM_SLP_S5_L	PM_SLP_S5_L - @m72_lib.M72	25D3 49C5 50A2
PM_STPCPU_L	PM_STPCPU_L - @m72_lib.M72	25C8 29C3 30C2
PM_STPPCI_L	PM_STPPCI_L - @m72_lib.M72	25C8 29C3 30C2
PM_SUS_STAT_L	PM_SUS_STAT_L - @m72_lib.M72	7C4 7D4 25D5 49C5 50A2
		51B4
PM_SYSRST_L	PM_SYSRST_L - @m72_lib.M72	7B8 25D5 28A3 49B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @m72_lib.M72	10C6 16A6 23C2 50C3 100B3
PM_THRM_L	PM_THRM_L - @m72_lib.M72	25C5
POWER_BUTTON_L	POWER_BUTTON_L - @m72_lib.M72	50C7
PP1V0_S5_FW_AVDD	PP1V0_S5_FW_AVDD - @m72_lib.M72	40D3 42A6 42D4
PP1V0_S5_FW_DVDD	PP1V0_S5_FW_DVDD - @m72_lib.M72	40D6 42B8 42C4
PP1V05_S0_NB_VCCPEG	PP1V05_S0_NB_VCCPEG - @m72_lib.M72	15D2 19B3 21D3
	PP1V05_S0_NB_VCCRXRDMI -	19B3 21C3
	@m72_lib.M72	
PP1V5_S0_NB_VCCD_TVD	PP1V5_S0_NB_VCCD_TVDAC -	19B6 22B1
AC	@m72_lib.M72	
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL -	26C3 27A6
L	@m72_lib.M72	
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL_F -	27A8
L_F	@m72_lib.M72	
PP1V5_S0_SB_VCCSATAP	PP1V5_S0_SB_VCCSATAPLL -	26B6 27A6
LL	@m72_lib.M72	
PP1V5_S0_SB_VCCSATAP	PP1V5_S0_SB_VCCSATAPLL_F -	27A8
LL_F	@m72_lib.M72	
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK - @m72_lib.M72	19B3 21A2
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK_RC -	21A4
_RC	@m72_lib.M72	
PP1V8_S3_R	PP1V8_S3_R - @m72_lib.M72	75C1
PP1V9R2V5_ENET_PHY_A	PP1V9R2V5_ENET_PHY_AVDD -	37C6 39D8 104B3
VDD	@m72_lib.M72	
PP1V9R2V5_S3_ENET_R	PP1V9R2V5_S3_ENET_R - @m72_lib.M72	38C3 104B2
	=YUKON_EC_PP2V5_ENET - @m72_lib.M72	37C7 38C1
PP1V25_S0M_NB_MPLL_R	PP1V25_S0M_NB_MPLL_RC -	21C3
C	@m72_lib.M72	
PP1V25_S0M_NB_VCCAXD	PP1V25_S0M_NB_VCCAXD - @m72_lib.M72	16A2 19C3 21A6
PP1V25_S0M_NB_VCCA_H	PP1V25_S0M_NB_VCCA_HPLL -	19D6 21D1
PLL	@m72_lib.M72	
PP1V25_S0M_NB_VCCA_M	PP1V25_S0M_NB_VCCA_MPLL -	19D6 21C1
PLL	@m72_lib.M72	
PP1V25_S0M_NB_VCCA_S	PP1V25_S0M_NB_VCCA_SM -	19C6 21B5
M	@m72_lib.M72	
PP1V25_S0M_NB_VCCA_S	PP1V25_S0M_NB_VCCA_SM_CK -	19B6 21B5
M_CK	@m72_lib.M72	
PP1V25_S0_NB_PEGPLL	PP1V25_S0_NB_PEGPLL - @m72_lib.M72	19C6 21B2
PP1V25_S0_NB_PEGPLL_	PP1V25_S0_NB_PEGPLL_RC -	21B4
RC	@m72_lib.M72	
PP1V25_S0_NB_VCCAXF	PP1V25_S0_NB_VCCAXF - @m72_lib.M72	19C3 21D3
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m72_lib.M72	39D7
PP3V3_FW_ESD	PP3V3_FW_ESD - @m72_lib.M72	43A6 43A6 43B6 43C5 43D5
PP3V3_G3_SB_RTC	PP3V3_G3_SB_RTC - @m72_lib.M72	23D7 26D6 27D5 28D5
PP3V3_S0M_CK505_VDD4	PP3V3_S0M_CK505_VDD48 -	29D4
8	@m72_lib.M72	
PP3V3_S0M_CK505_VDDA	PP3V3_S0M_CK505_VDDA - @m72_lib.M72	29C6
PP3V3_S0M_CK505_VDDA	PP3V3_S0M_CK505_VDDA_R -	29C7
_R	@m72_lib.M72	
PP3V3_S0M_CK505_VDD_	PP3V3_S0M_CK505_VDD_CPU_SRC -	29D7
CPU_SRC	@m72_lib.M72	
PP3V3_S0M_CK505_VDD_	PP3V3_S0M_CK505_VDD_PCI -	29D4
PCI	@m72_lib.M72	
PP3V3_S0M_CK505_VDD_	PP3V3_S0M_CK505_VDD_REF -	29C4
REF	@m72_lib.M72	
PP3V3_S0_CPUTHMSNS_R	PP3V3_S0_CPUTHMSNS_R - @m72_lib.M72	55D5
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @m72_lib.M72	71D7
PP3V3_S0_NB1V05_FOLL	PP3V3_S0_NB1V05_FOLLOW_R -	21C4
OW_R	@m72_lib.M72	
PP3V3_S0_NBCORE_FOLL	PP3V3_S0_NBCORE_FOLLOW_R -	21B4
OW_R	@m72_lib.M72	
PP3V3_S3_ENET_O	PP3V3_S3_ENET_O - @m72_lib.M72	38D6
PP3V3_S5_AVREF_SMC	PP3V3_S5_AVREF_SMC - @m72_lib.M72	49D4 50B7
PP3V3_S5_FW_AVDD1	PP3V3_S5_FW_AVDD1 - @m72_lib.M72	40D4 42A8 42B1
PP3V3_S5_FW_AVDD2	PP3V3_S5_FW_AVDD2 - @m72_lib.M72	40D3 42A7 42B1
PP3V3_S5_SMC_AVCC	PP3V3_S5_SMC_AVCC - @m72_lib.M72	49D3
PP5VREG_INTVCC	PP5VREG_INTVCC - @m72_lib.M72	76A2 76A6 76C3 76C6
PP5V_S0_DDC	PP5V_S0_DDC - @m72_lib.M72	94D3 94D4
PP5V_S0_DDC_DIODE	PP5V_S0_DDC_DIODE - @m72_lib.M72	94D6

PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m72_lib.M72	94D5
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @m72_lib.M72	71D7
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @m72_lib.M72	26D6 27C7
PP5V_S3_BNDI	PP5V_S3_BNDI - @m72_lib.M72	47B5 47D5
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @m72_lib.M72	26D6 27D7
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @m72_lib.M72	46B7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @m72_lib.M72	46B5
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @m72_lib.M72	46C7
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m72_lib.M72	46C5
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @m72_lib.M72	46D6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m72_lib.M72	46D2
PP12V_S3	PP12V_S3 - @m72_lib.M72	7D3 50B7 75D8 76D8 78D1
PPVBATT_G3_RTC	PPVBATT_G3_RTC - @m72_lib.M72	28D8
PPVBATT_G3_RTC_R	PPVBATT_G3_RTC_R - @m72_lib.M72	28D7
PPVIN_S0_P2V5S0_SVIN	PPVIN_S0_P2V5S0_SVIN - @m72_lib.M72	77C5
PPVIN_S5_5VS5_R	PPVIN_S5_5VS5_R - @m72_lib.M72	76C5
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m72_lib.M72	71D7
PPV_LCD_CONN	PPV_LCD_CONN - @m72_lib.M72	6A7 90A6 90A8 90C5
PPV_LCD_SW	PPV_LCD_SW - @m72_lib.M72	90C6
PPV_S0_LCD	PPV_S0_LCD - @m72_lib.M72	90C8
PPV_S0_MXM_PWRSRC	PPV_S0_MXM_PWRSRC - @m72_lib.M72	53C2 53D4 84C4
PPV_S3_ENET_O	PPV_S3_ENET_O - @m72_lib.M72	38B5
PPV_S3_ENET_R	PPV_S3_ENET_R - @m72_lib.M72	38B7
REMOTE_TEMP_ADDR	REMOTE_TEMP_ADDR - @m72_lib.M72	55A3
REMOTE_THRMD_M	REMOTE_THRMD_M - @m72_lib.M72	55A4
RSVD_EXTGPU_LVDS_EN	RSVD_EXTGPU_LVDS_EN - @m72_lib.M72	25D2
RSVD_MINI_BT_ACTIVE	RSVD_MINI_BT_ACTIVE - @m72_lib.M72	34C6
RSVD_MINI_WLAN_ACTIV	RSVD_MINI_WLAN_ACTIVE -	34C6
E	@m72_lib.M72	
RUNSS_GATE_D_L	RUNSS_GATE_D_L - @m72_lib.M72	70A7 70B7 70B7
SATA_A_D2R_C_N	SATA_A_D2R_C_N - @m72_lib.M72	45D7 103C3
SATA_A_D2R_C_P	SATA_A_D2R_C_P - @m72_lib.M72	45C7 103C3
SATA_A_D2R_N	SATA_A_D2R_N - @m72_lib.M72	7B8 23B6 45C5 103C3
SATA_A_D2R_P	SATA_A_D2R_P - @m72_lib.M72	7B8 23B6 45C5 103D3
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m72_lib.M72	23B6 45D5 103D3
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m72_lib.M72	23B6 45D5 103D3
SATA_A_R2D_N	SATA_A_R2D_N - @m72_lib.M72	45D7 103D3
SATA_A_R2D_P	SATA_A_R2D_P - @m72_lib.M72	45D7 103D3
SATA_B_D2R_N	SATA_B_D2R_N - @m72_lib.M72	23B6 45B7 103C3
	TP_SATA_B_D2R_N - @m72_lib.M72	45B5
SATA_B_D2R_P	SATA_B_D2R_P - @m72_lib.M72	23B6 45B7 103C3
	TP_SATA_B_D2R_P - @m72_lib.M72	45B5
SATA_B_DET_L	SATA_B_DET_L - @m72_lib.M72	25D3
SATA_B_PWR_EN_L	SATA_B_PWR_EN_L - @m72_lib.M72	25B5 25C5
SATA_B_R2D_C_N	SATA_B_R2D_C_N - @m72_lib.M72	23B6 45B5 103C3
	TP_SATA_B_R2D_N - @m72_lib.M72	45B7
SATA_B_R2D_C_P	SATA_B_R2D_C_P - @m72_lib.M72	23B6 45B5 103C3
	TP_SATA_B_R2D_P - @m72_lib.M72	45B7
SATA_C_D2R_N	SATA_C_D2R_N - @m72_lib.M72	23B6 45B7
	TP_SATA_C_D2R_N - @m72_lib.M72	45B5
SATA_C_D2R_P	SATA_C_D2R_P - @m72_lib.M72	23B6 45B7
	TP_SATA_C_D2R_P - @m72_lib.M72	45B5
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @m72_lib.M72	23B6 45B5
	TP_SATA_C_R2D_N - @m72_lib.M72	45B7
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @m72_lib.M72	23B6 45B5
	TP_SATA_C_R2D_P - @m72_lib.M72	45B7
SATA_RBIAS	SATA_RBIAS - @m72_lib.M72	45B2 103C3
	SATA_RBIAS_N - @m72_lib.M72	23B6 45B2
	SATA_RBIAS_P - @m72_lib.M72	23A6 45B2
	SATA_RBIAS_N - @m72_lib.M72	23B6 45B2
SB_A20GATE	SB_A20GATE - @m72_lib.M72	23C4
SB_CLINK_VREF0	SB_CLINK_VREF0 - @m72_lib.M72	25C3 104B3
SB_CLINK_VREF1	SB_CLINK_VREF1 - @m72_lib.M72	25C3 104B3
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @m72_lib.M72	7B8 25D3 30A6 105B3
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @m72_lib.M72	7B8 25D3 30C6 105B3
SB_CRT_TVOUT_MUX_L	SB_CRT_TVOUT_MUX_L - @m72_lib.M72	25D2 91A7
SB_GPIO10_CL1	SB_GPIO10_CL1 - @m72_lib.M72	25A5 25B3
SB_GPIO14_CL2	SB_GPIO14_CL2 - @m72_lib.M72	25A5 25B3
SB_GPIO18	SB_GPIO18 - @m72_lib.M72	25C5
SB_GPIO30	SB_GPIO30 - @m72_lib.M72	13C3 24C8
SB_GPIO36	SB_GPIO36 - @m72_lib.M72	25D3
SB_GPIO40	SB_GPIO40 - @m72_lib.M72	13C3 24C8
SB_INTVRMEN	SB_INTVRMEN - @m72_lib.M72	23D6
SB_LAN100_SLP	SB_LAN100_SLP - @m72_lib.M72	23C6
SB_RCIN_L	SB_RCIN_L - @m72_lib.M72	23C4
SB_RTC_RST_L	SB_RTC_RST_L - @m72_lib.M72	7B3 7B8 23D8 28D5
SB_RTC_X1	SB_RTC_X1 - @m72_lib.M72	23D8 28C8
SB_RTC_X1_R	SB_RTC_X1_R - @m72_lib.M72	28C7
SB_RTC_X2	SB_RTC_X2 - @m72_lib.M72	23D8 28C8
SB_SATALED_L	SB_SATALED_L - @m72_lib.M72	45C2
	TP_SB_SATALED_L - @m72_lib.M72	23B6 45C1
SB_SATALED_R_L	SB_SATALED_R_L - @m72_lib.M72	45C2
SB_SATA_CLKREQ_L	SB_SATA_CLKREQ_L - @m72_lib.M72	25C5 29B3 30D2
SB_SCLOCK	SB_SCLOCK - @m72_lib.M72	25C5
SB_SDATAOUT<0>	SB_SDATAOUT<0> - @m72_lib.M72	25C5
SB_SDATAOUT<1>	SB_SDATAOUT<1> - @m72_lib.M72	25C5
SB_SLOAD	SB_SLOAD - @m72_lib.M72	25C5
SB_SM_INTRUDER_L	SB_SM_INTRUDER_L - @m72_lib.M72	23D8 28D5
SB_SPKR	SB_SPKR - @m72_lib.M72	25B5
SDF3400_1	SDF3400_1 - @m72_lib.M72	34A5
SDF4720_1	SDF4720_1 - @m72_lib.M72	47C3
SDF4721_1	SDF4721_1 - @m72_lib.M72	47C2
SMBUS_SMC_0_S0_SCL	SMBUS_SMC_0_S0_SCL - @m72_lib.M72	52D5 106B3
	=SMB_AMB_TEMP_SCL - @m72_lib.M72	52D3 55C8
	=SMB_GPU_THRM_SCL - @m72_lib.M72	52D3 85C7
	SMB_0_S0_CLK - @m72_lib.M72	49B8 52D6
	=SMB_GPU_THRM_SCL - @m72_lib.M72	52D3 85C7
	=SMB_AMB_TEMP_SCL - @m72_lib.M72	52D3 55C8
SMBUS_SMC_0_S0_SDA	SMBUS_SMC_0_S0_SDA - @m72_lib.M72	52D5 106B3
	=SMB_AMB_TEMP_SDA - @m72_lib.M72	52C3 55C8
	=SMB_GPU_THRM_SDA - @m72_lib.M72	52D3 85C7
	SMB_0_S0_DATA - @m72_lib.M72	49B5 52D6
	=SMB_GPU_THRM_SDA - @m72_lib.M72	52D3 85C7
	=SMB_AMB_TEMP_SDA - @m72_lib.M72	52C3 55C8
SMBUS_SMC_A_S3_SCL	SMBUS_SMC_A_S3_SCL - @m72_lib.M72	106B3
SMBUS_SMC_A_S3_SDA	SMBUS_SMC_A_S3_SDA - @m72_lib.M72	106B3
SMBUS_SMC_A_S5_SCL	SMBUS_SMC_A_S5_SCL - @m72_lib.M72	52D2
	SMB_A_S3_CLK - @m72_lib.M72	49A5 52D3
SMBUS_SMC_A_S5_SDA	SMBUS_SMC_A_S5_SDA - @m72_lib.M72	52D2
	SMB_A_S3_DATA - @m72_lib.M72	49A5 52D3
SMBUS_SMC_BSA_SCL	SMBUS_SMC_BSA_SCL - @m72_lib.M72	52C2 106B3
	SMB_BSA_CLK - @m72_lib.M72	49A5 52C3
SMBUS_SMC_BSA_SDA	SMBUS_SMC_BSA_SDA - @m72_lib.M72	52C2 106B3
	SMB_BSA_DATA - @m72_lib.M72	49A5 52C3
SMBUS_SMC_B_S0_SCL	SMBUS_SMC_B_S0_SCL - @m72_lib.M72	52C5 106B3
	=SMBUS_MINI_SCL - @m72_lib.M72	34B3 52B3
	=SMB_REMOTE_TEMP_SCL - @m72_lib.M72	52C3 55B2
	=SMB_CPU_THRM_SCL - @m72_lib.M72	52C3 55C3
	SMB_B_S0_CLK - @m72_lib.M72	49A5 52C6
	=SMB_REMOTE_TEMP_SCL - @m72_lib.M72	52C3 55B2
	=SMB_CPU_THRM_SCL - @m72_lib.M72	52C3 55C3
	=SMBUS_MINI_SCL - @m72_lib.M72	34B3 52B3
SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA - @m72_lib.M72	52C5 106B3
	=SMBUS_MINI_SDA - @m72_lib.M72	34B3 52B3

	=SMB_REMOTE_TEMP_SDA - @m72_lib.M72	52B3 55B2
	=SMB_CPU_THRM_SDA - @m72_lib.M72	52C3 55C3
	SMB_B_S0_DATA - @m72_lib.M72	49A5 52C6
	=SMB_REMOTE_TEMP_SDA - @m72_lib.M72	52B3 55B2
	=SMB_CPU_THRM_SDA - @m72_lib.M72	52C3 55C3
	=SMBUS_MINI_SDA - @m72_lib.M72	34B3 52B3
SMBUS_SMC_MGMT_SCL	SMBUS_SMC_MGMT_SCL - @m72_lib.M72	52B2 106B3
	SMB_MGMT_CLK - @m72_lib.M72	49C5 52B3
SMBUS_SMC_MGMT_SDA	SMBUS_SMC_MGMT_SDA - @m72_lib.M72	52B2 106B3
	SMB_MGMT_DATA - @m72_lib.M72	49C8 52B3
SMB_CLK	SMB_CLK - @m72_lib.M72	25D5 52D8 103A3
	=SMBUS_CK505_SCL - @m72_lib.M72	29B5 52D6
	SMBUS_SB_SCL - @m72_lib.M72	52D7
	=I2C_DIMMA_SCL - @m72_lib.M72	31A6 52D6
	=I2C_DIMMB_SCL - @m72_lib.M72	32A6 52C6
	SMBUS_SB_SCL - @m72_lib.M72	52D7
	=SMBUS_CK505_SCL - @m72_lib.M72	29B5 52D6
	=I2C_DIMMB_SCL - @m72_lib.M72	32A6 52C6
	=I2C_DIMMA_SCL - @m72_lib.M72	31A6 52D6
SMB_DATA	SMB_DATA - @m72_lib.M72	25D5 52D8 103A3
	=SMBUS_CK505_SDA - @m72_lib.M72	29B5 52D6
	SMBUS_SB_SDA - @m72_lib.M72	52D7
	=I2C_DIMMA_SDA - @m72_lib.M72	31A6 52D6
	=I2C_DIMMB_SDA - @m72_lib.M72	32A6 52C6
	SMBUS_SB_SDA - @m72_lib.M72	52D7
	=SMBUS_CK505_SDA - @m72_lib.M72	29B5 52D6
	=I2C_DIMMB_SDA - @m72_lib.M72	32A6 52C6
	=I2C_DIMMA_SDA - @m72_lib.M72	31A6 52D6
SMB_ME_CLK	SMB_ME_CLK - @m72_lib.M72	25D5 52A8 103A3
	SMBUS_SB_ME_SCL - @m72_lib.M72	52A7
SMB_ME_DATA	SMB_ME_DATA - @m72_lib.M72	25D5 52A8 103A3
	SMBUS_SB_ME_SDA - @m72_lib.M72	52A7
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @m72_lib.M72	49D5 50C5
	TP_SMC_ADAPTER_EN - @m72_lib.M72	50C3
SMC_BATT_ISENSE	SMC_BATT_ISENSE - @m72_lib.M72	49C5 50B5
	SMC_NB_1V25_ISENSE - @m72_lib.M72	49C5 50B5
	UNUSED_SMC_SENSE - @m72_lib.M72	50A2 50B3 50B3 50B3 50B3
	SMC_PBUS_VSENSE - @m72_lib.M72	49C5 50B5
	SMC_DCIN_ISENSE - @m72_lib.M72	49C5 50B5
	UNUSED_SMC_SENSE - @m72_lib.M72	50A2 50B3 50B3 50B3 50B3
	SMC_PBUS_VSENSE - @m72_lib.M72	49C5 50B5
	SMC_NB_1V25_ISENSE - @m72_lib.M72	49C5 50B5
	SMC_DCIN_ISENSE - @m72_lib.M72	49C5 50B5
SMC_BC_ACOK	SMC_BC_ACOK - @m72_lib.M72	49C5 50B2
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @m72_lib.M72	49C5 50B2
SMC_CASE_OPEN	SMC_CASE_OPEN - @m72_lib.M72	49B5 50A2
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @m72_lib.M72	49C5 53C6
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @m72_lib.M72	49C5 53D6
SMC_EXCARD_CP	SMC_EXCARD_CP - @m72_lib.M72	49B8 50A2
SMC_EXCARD_OC_L	SMC_EXCARD_OC_L - @m72_lib.M72	49B8 50B2
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @m72_lib.M72	49B8 50B5
	TP_SMC_EXCARD_PWR_EN - @m72_lib.M72	50B3
SMC_EXTAL	SMC_EXTAL - @m72_lib.M72	49C3 50C8
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @m72_lib.M72	49A8 56D8
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @m72_lib.M72	49A8 56C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @m72_lib.M72	49A8 56B8
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @m72_lib.M72	49A8 56A8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @m72_lib.M72	49A8 57D8
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @m72_lib.M72	49A8 57C8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @m72_lib.M72	49A8 50C5
	TP_SMC_FAN_3_CTL - @m72_lib.M72	50C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @m72_lib.M72	49A8 50C5
	TP_SMC_FAN_3_TACH - @m72_lib.M72	50C3
SMC_FWE	SMC_FWE - @m72_lib.M72	49A5 50B2
SMC_GFX_OVERTEMP_L	SMC_GFX_OVERTEMP_L - @m72_lib.M72	49A8 85C8
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L - @m72_lib.M72	49C8 85B7
SMC_GPU_ISENSE	SMC_GPU_ISENSE - @m72_lib.M72	49C5 53C1
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @m72_lib.M72	49C5 53D2
SMC_KBC_MDE	SMC_KBC_MDE - @m72_lib.M72	49C2
SMC_LID	SMC_LID - @m72_lib.M72	49B5 50B2
SMC_LRESET_L	SMC_LRESET_L - @m72_lib.M72	7C6 28D1 49C8
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @m72_lib.M72	50D7
SMC_MD1	SMC_MD1 - @m72_lib.M72	7D4 49C1 51B6
SMC_MXM_VSENSE_R	SMC_MXM_VSENSE_R - @m72_lib.M72	53D3
SMC_NMI	SMC_NMI - @m72_lib.M72	7C4 49C1 51B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @m72_lib.M72	49B8 50B2
SMC_ONOFF_L	SMC_ONOFF_L - @m72_lib.M72	49C5 50B2 50C5
SMC_P14	SMC_P14 - @m72_lib.M72	49D8 50D5
	TP_SMC_P14 - @m72_lib.M72	50D3
SMC_P20	SMC_P20 - @m72_lib.M72	49C8 50D5
	TP_SMC_P20 - @m72_lib.M72	50D3
SMC_P21	SMC_P21 - @m72_lib.M72	49C8 50D5
	TP_SMC_P21 - @m72_lib.M72	50D3
SMC_P22	SMC_P22 - @m72_lib.M72	49C8 50C5
	TP_SMC_P22 - @m72_lib.M72	50C3
SMC_P23	SMC_P23 - @m72_lib.M72	49C8 50C5
	TP_SMC_P23 - @m72_lib.M72	50C3
SMC_P26	SMC_P26 - @m72_lib.M72	49C8 50C5
	TP_SMC_P26 - @m72_lib.M72	50C3
SMC_P27	SMC_P27 - @m72_lib.M72	49C8 50C5
	TP_SMC_P27 - @m72_lib.M72	50C3
SMC_P43	SMC_P43 - @m72_lib.M72	49C8 50C5
	TP_SMC_P43 - @m72_lib.M72	50C3
SMC_P44	SMC_P44 - @m72_lib.M72	49C8 50C5
	TP_SMC_P44 - @m72_lib.M72	50C3
SMC_P45	SMC_P45 - @m72_lib.M72	49C8 50C5
	TP_SMC_P45 - @m72_lib.M72	50C3
SMC_P46	SMC_P46 - @m72_lib.M72	49B8 50B5
	TP_SMC_P46 - @m72_lib.M72	50B3
SMC_P62	SMC_P62 - @m72_lib.M72	49D5 50C5
	TP_SMC_P62 - @m72_lib.M72	50C3
SMC_P63	SMC_P63 - @m72_lib.M72	49D5 50C5
	TP_SMC_P63 - @m72_lib.M72	50C3
SMC_P64	SMC_P64 - @m72_lib.M72	49D5 50C5
	TP_SMC_P64 - @m72_lib.M72	50C3
SMC_P67	SMC_P67 - @m72_lib.M72	49C5 50B2
SMC_P81	SMC_P81 - @m72_lib.M72	49C5 50C5
	TP_SMC_P81 - @m72_lib.M72	50C3
SMC_PA0	SMC_PA0 - @m72_lib.M72	49B8 50B2
SMC_PA1	SMC_PA1 - @m72_lib.M72	49B8 50B2
SMC_PB0	SMC_PB0 - @m72_lib.M72	49B8 50B2
SMC_PF0	SMC_PF0 - @m72_lib.M72	49B5 50C5
	TP_SMC_PF0 - @m72_lib.M72	50C3
SMC_PF1	SMC_PF1 - @m72_lib.M72	49B5 50C5
	TP_SMC_PF1 - @m72_lib.M72	50C3
SMC_PF3	SMC_PF3 - @m72_lib.M72	49B5 50B2
SMC_PG0	SMC_PG0 - @m72_lib.M72	49B5 50B2
SMC_PH4	SMC_PH4 - @m72_lib.M72	49A5 50B2
SMC_PM_G2_EN	SMC_PM_G2_EN - @m72_lib.M72	49D5 50C5
	TP_SMC_PM_G2_EN - @m72_lib.M72	50C3
SMC_PROCHOT	SMC_PROCHOT - @m72_lib.M72	49A5 50C1
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @m72_lib.M72	49C5 50D1
SMC_RESET_L	SMC_RESET_L - @m72_lib.M72	7C4 7C6 49C3 50D6 51B4
SMC_RSTGATE_L	SMC_RSTGATE_L - @m72_lib.M72	49D8 50B5

	TP_SMC_RSTGATE_L - @m72_lib.M72	50B3
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @m72_lib.M72	25C8 49B8
SMC_RX_L	SMC_RX_L - @m72_lib.M72	7C4 46D5 49B8 49C5 50B2
		51B4
SMC_SUS_CLK	SMC_SUS_CLK - @m72_lib.M72	49C5 50C3
	SUS_CLK_SB - @m72_lib.M72	25D3 50C2
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @m72_lib.M72	49B8 50B5
	TP_SMC_SYS_KBDLED - @m72_lib.M72	50B3
SMC_SYS_LED	SMC_SYS_LED - @m72_lib.M72	49C8 50A5 50A8
SMC_TCK	SMC_TCK - @m72_lib.M72	7D4 49B5 50B2 51B4
SMC_TDI	SMC_TDI - @m72_lib.M72	7D4 49B5 50B2 51B4
SMC_TDO	SMC_TDO - @m72_lib.M72	7D4 49B5 50B2 51B6
SMC_THRMTRIP	SMC_THRMTRIP - @m72_lib.M72	49A5 50C1
SMC_TMS	SMC_TMS - @m72_lib.M72	7D4 49B5 50B2 51B6
SMC_TRST_L	SMC_TRST_L - @m72_lib.M72	7D4 49C1 51B6
SMC_TX_L	SMC_TX_L - @m72_lib.M72	7D4 46D5 49B8 49C5 50B2
		51B6
SMC_VCL	SMC_VCL - @m72_lib.M72	49D2
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @m72_lib.M72	13C3 25C8 49C5
SMC_XTAL	SMC_XTAL - @m72_lib.M72	49C3 50C8
SMS_ONOFF_L	SMS_ONOFF_L - @m72_lib.M72	49A5 50B5
	TP_SMS_ONOFF_L - @m72_lib.M72	50B3
SMS_X_AXIS	SMS_X_AXIS - @m72_lib.M72	49A8 50D5 108D1
	NC_SMS_X_AXIS - @m72_lib.M72	50D3
SMS_Y_AXIS	SMS_Y_AXIS - @m72_lib.M72	49A8 50D5 108D1
	NC_SMS_Y_AXIS - @m72_lib.M72	50D3
SMS_Z_AXIS	SMS_Z_AXIS - @m72_lib.M72	49A8 50D5 108D1
	NC_SMS_Z_AXIS - @m72_lib.M72	50D3
SPI_A_SCLK_R	SPI_A_SCLK_R - @m72_lib.M72	103A3
SPI_A_SI_R	SPI_A_SI_R - @m72_lib.M72	61B4 103A3
SPI_A_SO_R	SPI_A_SO_R - @m72_lib.M72	7B3 61B4 103A3
SPI_B_SCLK_R	SPI_B_SCLK_R - @m72_lib.M72	103A3
SPI_B_SI_R	SPI_B_SI_R - @m72_lib.M72	103A3
SPI_B_SO	SPI_B_SO - @m72_lib.M72	103A3
SPI_B_SO_R	SPI_B_SO_R - @m72_lib.M72	103A3
SPI_CE_L<0>	SPI_CE_L<0> - @m72_lib.M72	7B3 61B6 103A3
SPI_CE_L<1>	SPI_CE_L<1> - @m72_lib.M72	103A3
SPI_CE_R_L<0>	SPI_CE_R_L<0> - @m72_lib.M72	24C5 61B7 103A3
SPI_CE_R_L<1>	SPI_CE_R_L<1> - @m72_lib.M72	103A3
SPI_HOLD_L	SPI_HOLD_L - @m72_lib.M72	61B5
SPI_SCLK	SPI_SCLK - @m72_lib.M72	7B3 61B6 103A3
SPI_SCLK_R	SPI_SCLK_R - @m72_lib.M72	7A8 24C5 61B7 103A3
SPI_SI	SPI_SI - @m72_lib.M72	103A3
SPI_SI_R	SPI_SI_R - @m72_lib.M72	24C5 61B3 103A3
SPI_SO	SPI_SO - @m72_lib.M72	7A8 24C5 61B3 103A3
SPI_WP_L	SPI_WP_L - @m72_lib.M72	61B5
SYSLED_SW	SYSLED_SW - @m72_lib.M72	50A4
SYS_LED_ANODE	SYS_LED_ANODE - @m72_lib.M72	50A6
SYS_LED_ANODE_CONN	SYS_LED_ANODE_CONN - @m72_lib.M72	50A3 50A4 50A5
SYS_LED_BIAS	SYS_LED_BIAS - @m72_lib.M72	50A7
SYS_LED_EN	SYS_LED_EN - @m72_lib.M72	50A8
SYS_LED_ILIM	SYS_LED_ILIM - @m72_lib.M72	50A6
SYS_LED_IREF	SYS_LED_IREF - @m72_lib.M72	50A7
SYS_LED_RETURN_CONN	SYS_LED_RETURN_CONN - @m72_lib.M72	50A3 50A4 50A5
SYS_LGP_ANODE	SYS_LGP_ANODE - @m72_lib.M72	50A4
SYS_LGP_RETURN	SYS_LGP_RETURN - @m72_lib.M72	50A4
SYS_ONEWIRE	SYS_ONEWIRE - @m72_lib.M72	49B8 50B2
TMDS_CLK_N	TMDS_CLK_N - @m72_lib.M72	85A7 94C8 108D3
TMDS_CLK_P	TMDS_CLK_P - @m72_lib.M72	85A7 94B8 108D3
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m72_lib.M72	94C4 94C7 108D3
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m72_lib.M72	94B7 94C4 108D3
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m72_lib.M72	94C4 94D6
TMDS_CONN_DN<3..0>	TMDS_CONN_DN<3..0> - @m72_lib.M72	108D3
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m72_lib.M72	94C4 94D6
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m72_lib.M72	94C6 94D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m72_lib.M72	94C4 94D6
TMDS_CONN_DP<3..0>	TMDS_CONN_DP<3..0> - @m72_lib.M72	108D3
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m72_lib.M72	94C4 94D6
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m72_lib.M72	94C6 94D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m72_lib.M72	85A7 94D8
TMDS_DATA_N<3..0>	TMDS_DATA_N<3..0> - @m72_lib.M72	108D3
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m72_lib.M72	85A7 94D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m72_lib.M72	85A7 94C8
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m72_lib.M72	85A7 94D8
TMDS_DATA_P<3..0>	TMDS_DATA_P<3..0> - @m72_lib.M72	108D3
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m72_lib.M72	85A7 94C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m72_lib.M72	85A7 94C8
TP_CK505_PGMODE	TP_CK505_PGMODE - @m72_lib.M72	7D2 29B5
TP_CPU_RSVD0	TP_CPU_RSVD0 - @m72_lib.M72	10B8
TP_CPU_RSVD1	TP_CPU_RSVD1 - @m72_lib.M72	10B8
TP_CPU_RSVD2	TP_CPU_RSVD2 - @m72_lib.M72	10B8
TP_CPU_RSVD3	TP_CPU_RSVD3 - @m72_lib.M72	10B8
TP_CPU_RSVD4	TP_CPU_RSVD4 - @m72_lib.M72	10B8
TP_CPU_RSVD5	TP_CPU_RSVD5 - @m72_lib.M72	10B8
TP_CPU_RSVD6	TP_CPU_RSVD6 - @m72_lib.M72	10B8
TP_CPU_RSVD7	TP_CPU_RSVD7 - @m72_lib.M72	10B8
TP_CPU_RSVD8	TP_CPU_RSVD8 - @m72_lib.M72	10B8
TP_CPU_RSVD9	TP_CPU_RSVD9 - @m72_lib.M72	10B8
TP_CPU_TEST3	TP_CPU_TEST3 - @m72_lib.M72	10B4
TP_CPU_TEST5	TP_CPU_TEST5 - @m72_lib.M72	10B4
TP_CPU_TEST6	TP_CPU_TEST6 - @m72_lib.M72	10B4
TP_ENET_GLAN_CLK	TP_ENET_GLAN_CLK - @m72_lib.M72	23C6
TP_FW_AVREG	TP_FW_AVREG - @m72_lib.M72	40B6
TP_FW_CE	TP_FW_CE - @m72_lib.M72	7B3 40B6
TP_FW_FW620_L	TP_FW_FW620_L - @m72_lib.M72	40B6
TP_FW_JASI_EN	TP_FW_JASI_EN - @m72_lib.M72	40B6
TP_FW_MODE_A	TP_FW_MODE_A - @m72_lib.M72	40B6
TP_FW_NAND_TREE	TP_FW_NAND_TREE - @m72_lib.M72	7C3 40B6
TP_FW_SCIFCLK	TP_FW_SCIFCLK - @m72_lib.M72	40B3
TP_FW_SCIFDAIN	TP_FW_SCIFDAIN - @m72_lib.M72	40B3
TP_FW_SCIFDOUT	TP_FW_SCIFDOUT - @m72_lib.M72	40B3
TP_FW_SCIFMC	TP_FW_SCIFMC - @m72_lib.M72	40B3
TP_FW_SDA	TP_FW_SDA - @m72_lib.M72	40B3
TP_FW_SE	TP_FW_SE - @m72_lib.M72	7C3 40B6
TP_FW_SM	TP_FW_SM - @m72_lib.M72	7C3 40B6
TP_FW_TCK	TP_FW_TCK - @m72_lib.M72	7C3 40C3
TP_FW_TDI	TP_FW_TDI - @m72_lib.M72	7C3 40C3
TP_FW_TDO	TP_FW_TDO - @m72_lib.M72	7C3 40C3
TP_FW_TMS	TP_FW_TMS - @m72_lib.M72	7C3 40C3
TP_FW_VAUX_DISABLE	TP_FW_VAUX_DISABLE - @m72_lib.M72	40C3
TP_FW_VBUF	TP_FW_VBUF - @m72_lib.M72	40B6
TP_GPU_DDC_B_CLK	TP_GPU_DDC_B_CLK - @m72_lib.M72	85A4
TP_GPU_DDC_B_DATA	TP_GPU_DDC_B_DATA - @m72_lib.M72	85A4
TP_HDA_DOCK_RST_L	TP_HDA_DOCK_RST_L - @m72_lib.M72	23B6
TP_HDA_SDIN1	TP_HDA_SDIN1 - @m72_lib.M72	23C8
TP_HDA_SDIN2	TP_HDA_SDIN2 - @m72_lib.M72	23C8
TP_HDA_SDIN3	TP_HDA_SDIN3 - @m72_lib.M72	23C8
TP_LAN_D2R<0>	TP_LAN_D2R<0> - @m72_lib.M72	23C6
TP_LAN_D2R<1>	TP_LAN_D2R<1> - @m72_lib.M72	23C6
TP_LAN_D2R<2>	TP_LAN_D2R<2> - @m72_lib.M72	7D2 23C6 28C4
TP_LAN_R2D<0>	TP_LAN_R2D<0> - @m72_lib.M72	23C6
TP_LAN_R2D<1>	TP_LAN_R2D<1> - @m72_lib.M72	23C6
TP_LAN_R2D<2>	TP_LAN_R2D<2> - @m72_lib.M72	23C6
TP_LAN_RSTSYNC	TP_LAN_RSTSYNC - @m72_lib.M72	23C6

TP_LPC_DRQ0_L	TP_LPC_DRQ0_L - @m72_lib.M72	23D4
TP_LVDS_A_DATAN3	TP_LVDS_A_DATAN3 - @m72_lib.M72	16C6
TP_LVDS_A_DATAP3	TP_LVDS_A_DATAP3 - @m72_lib.M72	16C6
TP_LVDS_B_DATAN3	TP_LVDS_B_DATAN3 - @m72_lib.M72	16C6
TP_LVDS_B_DATAP3	TP_LVDS_B_DATAP3 - @m72_lib.M72	16C6
TP_LVDS_VBG	TP_LVDS_VBG - @m72_lib.M72	15D5
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m72_lib.M72	31C3
TP_MEM_A_RCVEN_L	TP_MEM_A_RCVEN_L - @m72_lib.M72	17B5
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m72_lib.M72	32C3
TP_MEM_B_RCVEN_L	TP_MEM_B_RCVEN_L - @m72_lib.M72	17B2
TP_MEM_CLKN2	TP_MEM_CLKN2 - @m72_lib.M72	16C6
TP_MEM_CLKN5	TP_MEM_CLKN5 - @m72_lib.M72	16C6
TP_MEM_CLKP2	TP_MEM_CLKP2 - @m72_lib.M72	16C6
TP_MEM_CLKP5	TP_MEM_CLKP5 - @m72_lib.M72	16C6
TP_NB_CFG<10>	TP_NB_CFG<10> - @m72_lib.M72	16B6
TP_NB_CFG<11>	TP_NB_CFG<11> - @m72_lib.M72	16B6
TP_NB_CFG<12>	TP_NB_CFG<12> - @m72_lib.M72	7C3 16B6
TP_NB_CFG<13>	TP_NB_CFG<13> - @m72_lib.M72	7C3 16B6
TP_NB_CFG<14>	TP_NB_CFG<14> - @m72_lib.M72	16B6
TP_NB_CFG<15>	TP_NB_CFG<15> - @m72_lib.M72	16B6
TP_NB_CFG<17>	TP_NB_CFG<17> - @m72_lib.M72	16B6
TP_NB_CFG<18>	TP_NB_CFG<18> - @m72_lib.M72	7C3 16B6
TP_NB_NC<1>	TP_NB_NC<1> - @m72_lib.M72	7D2 16A6
TP_NB_NC<2>	TP_NB_NC<2> - @m72_lib.M72	7D2 16A6
TP_NB_NC<3>	TP_NB_NC<3> - @m72_lib.M72	7D2 16A6
TP_NB_NC<4>	TP_NB_NC<4> - @m72_lib.M72	7D2 16A6
TP_NB_NC<5>	TP_NB_NC<5> - @m72_lib.M72	7D2 16A6
TP_NB_NC<6>	TP_NB_NC<6> - @m72_lib.M72	16A6
TP_NB_NC<7>	TP_NB_NC<7> - @m72_lib.M72	16A6
TP_NB_NC<8>	TP_NB_NC<8> - @m72_lib.M72	16A6
TP_NB_NC<9>	TP_NB_NC<9> - @m72_lib.M72	16A6
TP_NB_NC<10>	TP_NB_NC<10> - @m72_lib.M72	16A6
TP_NB_NC<11>	TP_NB_NC<11> - @m72_lib.M72	16A6
TP_NB_NC<12>	TP_NB_NC<12> - @m72_lib.M72	16A6
TP_NB_NC<13>	TP_NB_NC<13> - @m72_lib.M72	16A6
TP_NB_NC<14>	TP_NB_NC<14> - @m72_lib.M72	16A6
TP_NB_NC<15>	TP_NB_NC<15> - @m72_lib.M72	16A6
TP_NB_NC<16>	TP_NB_NC<16> - @m72_lib.M72	16A6
TP_NB_RSVD<1>	TP_NB_RSVD<1> - @m72_lib.M72	16D6
TP_NB_RSVD<2>	TP_NB_RSVD<2> - @m72_lib.M72	16D6
TP_NB_RSVD<3>	TP_NB_RSVD<3> - @m72_lib.M72	16D6
TP_NB_RSVD<4>	TP_NB_RSVD<4> - @m72_lib.M72	16D6
TP_NB_RSVD<5>	TP_NB_RSVD<5> - @m72_lib.M72	16D6
TP_NB_RSVD<6>	TP_NB_RSVD<6> - @m72_lib.M72	16D6
TP_NB_RSVD<7>	TP_NB_RSVD<7> - @m72_lib.M72	16D6
TP_NB_RSVD<8>	TP_NB_RSVD<8> - @m72_lib.M72	16D6
TP_NB_RSVD<9>	TP_NB_RSVD<9> - @m72_lib.M72	16D6
TP_NB_RSVD<10>	TP_NB_RSVD<10> - @m72_lib.M72	7B3 16D6
TP_NB_RSVD<11>	TP_NB_RSVD<11> - @m72_lib.M72	7B3 16D6
TP_NB_RSVD<12>	TP_NB_RSVD<12> - @m72_lib.M72	7B3 16D6
TP_NB_RSVD<13>	TP_NB_RSVD<13> - @m72_lib.M72	7B3 16D6
TP_NB_RSVD<14>	TP_NB_RSVD<14> - @m72_lib.M72	16D6
TP_NB_RSVD<20>	TP_NB_RSVD<20> - @m72_lib.M72	16D6
TP_NB_RSVD<21>	TP_NB_RSVD<21> - @m72_lib.M72	16D6
TP_NB_RSVD<22>	TP_NB_RSVD<22> - @m72_lib.M72	16C6
TP_NB_RSVD<23>	TP_NB_RSVD<23> - @m72_lib.M72	16C6
TP_NB_RSVD<24>	TP_NB_RSVD<24> - @m72_lib.M72	16C6
TP_NB_RSVD<25>	TP_NB_RSVD<25> - @m72_lib.M72	16C6
TP_NB_RSVD<26>	TP_NB_RSVD<26> - @m72_lib.M72	16C6
TP_NB_RSVD<27>	TP_NB_RSVD<27> - @m72_lib.M72	16C6
TP_NB_RSVD<34>	TP_NB_RSVD<34> - @m72_lib.M72	16C6
TP_NB_RSVD<35>	TP_NB_RSVD<35> - @m72_lib.M72	16C6
TP_NB_RSVD<36>	TP_NB_RSVD<36> - @m72_lib.M72	16C6
TP_NB_RSVD<41>	TP_NB_RSVD<41> - @m72_lib.M72	16C6
TP_NB_RSVD<42>	TP_NB_RSVD<42> - @m72_lib.M72	16C6
TP_NB_RSVD<43>	TP_NB_RSVD<43> - @m72_lib.M72	16C6
TP_NB_RSVD<44>	TP_NB_RSVD<44> - @m72_lib.M72	16C6
TP_NB_RSVD<45>	TP_NB_RSVD<45> - @m72_lib.M72	16C6
TP_PCIE_A_D2R_N	TP_PCIE_A_D2R_N - @m72_lib.M72	24D5
TP_PCIE_A_D2R_P	TP_PCIE_A_D2R_P - @m72_lib.M72	24D5
TP_PCIE_A_R2D_C_N	TP_PCIE_A_R2D_C_N - @m72_lib.M72	24D5
TP_PCIE_A_R2D_C_P	TP_PCIE_A_R2D_C_P - @m72_lib.M72	24D5
TP_PCIE_B_D2R_N	TP_PCIE_B_D2R_N - @m72_lib.M72	24D5
TP_PCIE_B_D2R_P	TP_PCIE_B_D2R_P - @m72_lib.M72	24D5
TP_PCIE_B_R2D_C_N	TP_PCIE_B_R2D_C_N - @m72_lib.M72	24D5
TP_PCIE_B_R2D_C_P	TP_PCIE_B_R2D_C_P - @m72_lib.M72	24D5
TP_PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N - @m72_lib.M72	24D5
TP_PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P - @m72_lib.M72	24D5
TP_PCIE_EXCARD_R2D_C	TP_PCIE_EXCARD_R2D_C_N -	24D5
_N	@m72_lib.M72	
TP_PCIE_EXCARD_R2D_C	TP_PCIE_EXCARD_R2D_C_P -	24D5
_P	@m72_lib.M72	
TP_PCI_PME_L	TP_PCI_PME_L - @m72_lib.M72	24A6
TP_PM_SLP_M_L	TP_PM_SLP_M_L - @m72_lib.M72	25C3
TP_PM_SLP_S4_L	TP_PM_SLP_S4_L - @m72_lib.M72	25D3
TP_PP5VREG_PLLIN	TP_PP5VREG_PLLIN - @m72_lib.M72	76B5
TP_SB_GPIO51	TP_SB_GPIO51 - @m72_lib.M72	24B6
TP_SB_GPIO53	TP_SB_GPIO53 - @m72_lib.M72	24B6
TP_SB_GPIO55	TP_SB_GPIO55 - @m72_lib.M72	24B6
TP_SB_TP3	TP_SB_TP3 - @m72_lib.M72	25B5
TP_SB_TP7	TP_SB_TP7 - @m72_lib.M72	25C5
TP_SB_TP8	TP_SB_TP8 - @m72_lib.M72	23C4
TP_SPI_CE_R_L<1>	TP_SPI_CE_R_L<1> - @m72_lib.M72	24C5
TP_VCCCL1_05_INTERNA	TP_VCCCL1_05_INTERNAL_REG -	26A3
L_REG	@m72_lib.M72	
TP_VCCLAN1_05_INTERN	TP_VCCLAN1_05_INTERNAL_REG1 -	26A6
AL_REG1	@m72_lib.M72	
TP_VCCLAN1_05_INTERN	TP_VCCLAN1_05_INTERNAL_REG2 -	26A6
AL_REG2	@m72_lib.M72	
TP_VCCSUS1_05_INTERN	TP_VCCSUS1_05_INTERNAL_REG1 -	26B3
AL_REG1	@m72_lib.M72	
TP_VCCSUS1_05_INTERN	TP_VCCSUS1_05_INTERNAL_REG2 -	26B3
AL_REG2	@m72_lib.M72	
TP_VCCSUS1_5_INTERNA	TP_VCCSUS1_5_INTERNAL_REG1 -	26B3
L_REG1	@m72_lib.M72	
TP_VCCSUS1_5_INTERNA	TP_VCCSUS1_5_INTERNAL_REG2 -	26B3
L_REG2	@m72_lib.M72	
TP_XDP_HOOK2	TP_XDP_HOOK2 - @m72_lib.M72	13B6
TP_XDP_HOOK3	TP_XDP_HOOK3 - @m72_lib.M72	13B6
U5500_TCRIT1	U5500_TCRIT1 - @m72_lib.M72	55B3
U5500_TCRIT2	U5500_TCRIT2 - @m72_lib.M72	55B3
U5500_TCRIT3	U5500_TCRIT3 - @m72_lib.M72	55A3
U7550_VDDQ	U7550_VDDQ - @m72_lib.M72	75B5
USB_BT_N	USB_BT_N - @m72_lib.M72	7A8 24C2 47D3 103B3
USB_BT_P	USB_BT_P - @m72_lib.M72	7A8 24C2 47C3 103B3
USB_CAMERA_L_N	USB_CAMERA_L_N - @m72_lib.M72	47B5 108C3
USB_CAMERA_L_P	USB_CAMERA_L_P - @m72_lib.M72	47B5 108C3
USB_CAMERA_N	USB_CAMERA_N - @m72_lib.M72	7A8 24C2 47B7 103B3
USB_CAMERA_P	USB_CAMERA_P - @m72_lib.M72	7A8 24C2 47B7 103B3
USB_C_MUXED_N	USB_C_MUXED_N - @m72_lib.M72	46D3 108C3
USB_C_MUXED_P	USB_C_MUXED_P - @m72_lib.M72	46D3 108D3
USB_DEBUGPRT_EN_L	USB_DEBUGPRT_EN_L - @m72_lib.M72	46C4 49B8
USB_EXCARD_N	USB_EXCARD_N - @m72_lib.M72	24C2 47B3 103B3
	TP_USB_EXCARD_N - @m72_lib.M72	47B1

USB_EXCARD_P	USB_EXCARD_P - @m72_lib.M72	24C2 47B3 103B3
	TP_USB_EXCARD_P - @m72_lib.M72	47B1
USB_EXTA_MUXED_N	USB_EXTA_MUXED_N - @m72_lib.M72	103B3
USB_EXTA_MUXED_P	USB_EXTA_MUXED_P - @m72_lib.M72	103B3
USB_EXTA_N	USB_EXTA_N - @m72_lib.M72	24C2 46A7 103B3
USB_EXTA_OC_L	USB_EXTA_OC_L - @m72_lib.M72	13C3 24C8 46C8
USB_EXTA_P	USB_EXTA_P - @m72_lib.M72	24C2 46A7 103B3
USB_EXTB_N	USB_EXTB_N - @m72_lib.M72	24C2 46B7 103B3
USB_EXTB_OC_L	USB_EXTB_OC_L - @m72_lib.M72	13C3 24C8 46C8
USB_EXTB_P	USB_EXTB_P - @m72_lib.M72	24C2 46B7 103B3
USB_EXTC_N	USB_EXTC_N - @m72_lib.M72	24C2 46D5 103A3
USB_EXTC_OC_L	USB_EXTC_OC_L - @m72_lib.M72	24C8 46D8
USB_EXTC_P	USB_EXTC_P - @m72_lib.M72	24C2 46D5 103B3
USB_EXTD_N	USB_EXTD_N - @m72_lib.M72	24C2 46B3 103B3
	TP_USB_EXTD_N - @m72_lib.M72	46B2
USB_EXTD_OC_L	USB_EXTD_OC_L - @m72_lib.M72	13C3 24C8
USB_EXTD_P	USB_EXTD_P - @m72_lib.M72	24C2 46B3 103B3
	TP_USB_EXTD_P - @m72_lib.M72	46B2
USB_IR_L_N	USB_IR_L_N - @m72_lib.M72	47A5 58C5 108C3
USB_IR_L_P	USB_IR_L_P - @m72_lib.M72	47A5 58C5 108C3
USB_IR_N	USB_IR_N - @m72_lib.M72	7A8 24C2 47A7 103B3
USB_IR_P	USB_IR_P - @m72_lib.M72	7A8 24C2 47A7 103B3
USB_MINI_N	USB_MINI_N - @m72_lib.M72	24C2 34B3 103B3
USB_MINI_P	USB_MINI_P - @m72_lib.M72	24C2 34B3 103B3
USB_PORT0_N	USB_PORT0_N - @m72_lib.M72	46A5 108D3
USB_PORT0_P	USB_PORT0_P - @m72_lib.M72	46A5 108D3
USB_PORT1_N	USB_PORT1_N - @m72_lib.M72	46B5 108D3
USB_PORT1_P	USB_PORT1_P - @m72_lib.M72	46B5 108D3
USB_PORT2_N	USB_PORT2_N - @m72_lib.M72	46D2 108D3
USB_PORT2_P	USB_PORT2_P - @m72_lib.M72	46D2 108D3
USB_PWR_ENA_L	USB_PWR_ENA_L - @m72_lib.M72	46D8
USB_RBIAS	USB_RBIAS - @m72_lib.M72	24B3 103A3
USB_TPAD_N	USB_TPAD_N - @m72_lib.M72	24C2 47B3 103B3
	TP_USB_TPAD_N - @m72_lib.M72	47B2
USB_TPAD_P	USB_TPAD_P - @m72_lib.M72	24C2 47B3 103B3
	TP_USB_TPAD_P - @m72_lib.M72	47B2
VCCCL1_5V	VCCCL1_5V - @m72_lib.M72	26A4
VGA_BLU	VGA_BLU - @m72_lib.M72	91A4 94C5 108A3
VGA_GRN	VGA_GRN - @m72_lib.M72	91B4 94C5 108A3
VGA_HSYNC	VGA_HSYNC - @m72_lib.M72	91A2 94C5 108A3
VGA_HSYNC_R	VGA_HSYNC_R - @m72_lib.M72	91A3
VGA_RED	VGA_RED - @m72_lib.M72	91B4 94C5 108A3
VGA_VSYNC	VGA_VSYNC - @m72_lib.M72	91B2 94C5 108A3
VGA_VSYNC_R	VGA_VSYNC_R - @m72_lib.M72	91B3
VIDEO_MUX_BLU	VIDEO_MUX_BLU - @m72_lib.M72	91B7 108A3
VIDEO_MUX_GRN	VIDEO_MUX_GRN - @m72_lib.M72	91B7 108A3
VIDEO_MUX_RED	VIDEO_MUX_RED - @m72_lib.M72	91B7 108A3
VR_PWRGD_CLKEN	VR_PWRGD_CLKEN - @m72_lib.M72	7C4 25C5 28A6
VR_PWRGD_CLKEN_L	VR_PWRGD_CLKEN_L - @m72_lib.M72	28A8 71C7
WOL_EN	WOL_EN - @m72_lib.M72	25B3
WOW_EN	WOW_EN - @m72_lib.M72	13C3 24C8
XDP_BPM_L<0>	XDP_BPM_L<0> - @m72_lib.M72	10C6 13C6
XDP_BPM_L<4..0>	XDP_BPM_L<4..0> - @m72_lib.M72	100A3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m72_lib.M72	10C6 13C6
XDP_BPM_L<2>	XDP_BPM_L<2> - @m72_lib.M72	10C6 13C6
XDP_BPM_L<3>	XDP_BPM_L<3> - @m72_lib.M72	10C6 13C6
XDP_BPM_L<4>	XDP_BPM_L<4> - @m72_lib.M72	10C6 13C6
XDP_BPM_L<5>	XDP_BPM_L<5> - @m72_lib.M72	10C5 13C6 100A3
XDP_CPURST_L	XDP_CPURST_L - @m72_lib.M72	13B4
XDP_DBRESET_L	XDP_DBRESET_L - @m72_lib.M72	10C6 13B3 28A5
XDP_OBS20	XDP_OBS20 - @m72_lib.M72	13B6
XDP_PWRGD	XDP_PWRGD - @m72_lib.M72	13C6
XDP_TCK	XDP_TCK - @m72_lib.M72	10A7 10C6 13B6 100A3
XDP_TDI	XDP_TDI - @m72_lib.M72	10B7 10C6 13B3 100A3
XDP_TDO	XDP_TDO - @m72_lib.M72	10A7 10C6 13B3 100A3
XDP_TMS	XDP_TMS - @m72_lib.M72	10B7 10C6 13B3 100A3
XDP_TRST_L	XDP_TRST_L - @m72_lib.M72	10A7 10C6 13B3 100A3
YUKON_RSET	YUKON_RSET - @m72_lib.M72	37C2
YUKON_VPD_CLK	YUKON_VPD_CLK - @m72_lib.M72	37B2
YUKON_VPD_DATA	YUKON_VPD_DATA - @m72_lib.M72	37B2

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C600	CAP_402	m72[6D7]
C621	CAP_603	m72[6D6]
C622	CAP_805	m72[6D7]
C623	CAP_805	m72[6D7]
C624	CAP_1210	m72[6D8]
C625	CAP_P_6.3X5.5-SM	m72[6D8]
C1000	CAP_402	m72[10B5]
C1200	CAP_805	m72[12D7]
C1201	CAP_805	m72[12D6]
C1202	CAP_805	m72[12D6]
C1203	CAP_805	m72[12D6]
C1204	CAP_805	m72[12D6]
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C1209	CAP_805	m72[12D4]
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C1223	CAP_805	m72[12C6]
C1224	CAP_805	m72[12C6]
C1225	CAP_805	m72[12C5]
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C1227	CAP_805	m72[12B6]
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C1229	CAP_805	m72[12B6]
C1230	CAP_805	m72[12B6]
C1231	CAP_805	m72[12B5]
C1235	CAP_P_6.3X8-SM	m72[12A3]
C1236	CAP_402	m72[12A2]
C1237	CAP_402	m72[12A2]
C1238	CAP_402	m72[12A2]
C1239	CAP_402	m72[12A2]
C1240	CAP_402	m72[12A1]
C1241	CAP_402	m72[12A1]
C1250	CAP_P_CASE-D2-SM1	m72[12B7]
C1251	CAP_P_CASE-D2-SM1	m72[12B6]
C1252	CAP_P_CASE-D2-SM1	m72[12B5]
C1253	CAP_P_CASE-D2-SM1	m72[12B5]
C1254	CAP_P_CASE-D2-SM1	m72[12B6]
C1255	CAP_P_CASE-D2-SM1	m72[12B5]
C1280	CAP_603	m72[12B3]
C1281	CAP_402	m72[12B2]
C1300	CAP_402	m72[13B5]
C1301	CAP_402	m72[13B4]
C1410	CAP_402	m72[14A6]
C1425	CAP_402	m72[14A7]
C1615	CAP_402	m72[16C3]
C1616	CAP_402	m72[16C3]
C1622	CAP_603	m72[16C1]
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C1624	CAP_603	m72[16C1]
C1625	CAP_402	m72[16C1]
C1640	CAP_402	m72[16A3]
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C1807	CAP_402	m72[18A5]
C1911	CAP_402	m72[19A3]
C1912	CAP_402	m72[19A3]
C1913	CAP_402	m72[19A3]
C2100	CAP_P_6.3X8-SM	m72[21D7]
C2101	CAP_805	m72[21D7]
C2102	CAP_402	m72[21D7]
C2103	CAP_402	m72[21D6]
C2104	CAP_402	m72[21D6]
C2110	CAP_805	m72[21C7]
C2111	CAP_402	m72[21C7]
C2112	CAP_402	m72[21C7]
C2113	CAP_402	m72[21C6]
C2114	CAP_402	m72[21C6]
C2115	CAP_402	m72[21C6]
C2120	CAP_P_6.3X8-SM	m72[21C7]
C2121	CAP_603	m72[21C7]
C2122	CAP_603	m72[21C7]
C2123	CAP_603	m72[21C6]
C2124	CAP_402	m72[21C6]
C2130	CAP_P_6.3X8-SM	m72[21C7]
C2131	CAP_805	m72[21C7]
C2132	CAP_805	m72[21C7]
C2135	CAP_402	m72[21C7]
C2140	CAP_P_6.3X8-SM	m72[21B7]
C2141	CAP_805	m72[21B7]
C2142	CAP_805	m72[21B6]
C2143	CAP_603	m72[21B6]
C2144	CAP_402-1	m72[21B6]
C2145	CAP_805	m72[21B6]
C2146	CAP_603	m72[21B6]
C2148	CAP_402	m72[21B6]
C2150	CAP_805	m72[21A7]
C2151	CAP_402-1	m72[21A6]
C2160	CAP_402	m72[21A7]
C2161	CAP_402	m72[21A7]
C2165	CAP_402	m72[21A7]
C2170	CAP_603	m72[21D4]
C2171	CAP_402-1	m72[21D4]
C2173	CAP_P_SM-CASE-C1	m72[21C4]
C2174	CAP_603	m72[21C4]
C2177	CAP_603	m72[21C4]
C2180	CAP_402	m72[21D2]
C2181	CAP_805	m72[21D2]
C2182	CAP_402	m72[21D2]
C2183	CAP_805	m72[21C3]
C2184	CAP_402	m72[21C2]
C2190	CAP_603	m72[21B4]
C2191	CAP_402	m72[21B3]
C2192	CAP_402	m72[21B3]
C2195	CAP_603	m72[21A4]
C2196	CAP_805	m72[21A3]
C2197	CAP_402	m72[21A3]
C2200	CAP_402	m72[22B2]
C2201	FILTER_3P_A_NFM18	m72[22B2]
C2213	CAP_603	m72[22B2]
C2500	CAP_402	m72[25C2]
C2501	CAP_402	m72[25B2]
C2600	CAP_402	m72[26A3]
C2601	CAP_402	m72[26A3]
C2700	CAP_P_SM-CASE-C1	m72[27C7]
C2701	CAP_402	m72[27A6]
C2702	CAP_402	m72[27B1]
C2703	CAP_402	m72[27C8]
C2704	CAP_402	m72[27D8]
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C2706	CAP_805	m72[27C7]
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C2719	CAP_402	m72[27D3]
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C2731	CAP_402	m72[27D5]
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C2733	CAP_603	m72[27C5]
C2734	CAP_402	m72[27D5]
C2735	CAP_603	m72[27A6]
C2736	CAP_603	m72[27B7]
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C2738	CAP_402	m72[27C3]
C2739	CAP_805	m72[27C1]
C2741	CAP_402	m72[27B3]
C2805	CAP_402	m72[28D5]
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C2810	CAP_402	m72[28D6]
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C2910	CAP_603	m72[29D3]
C2911	CAP_402	m72[29D2]
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C2913	CAP_402	m72[29D3]
C2914	CAP_603	m72[29D3]
C2915	CAP_402	m72[29C4]
C2916	CAP_603	m72[29C3]
C2989	CAP_402	m72[29C6]
C2990	CAP_402	m72[29C6]
C3100	CAP_603	m72[31B2]
C3101	CAP_603	m72[31B2]
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C3112	CAP_402	m72[31B1]
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C3130	CAP_603	m72[31D6]
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C3140	CAP_603	m72[31A7]
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C3230	CAP_603	m72[32D6]
C3231	CAP_402	m72[32D6]
C3240	CAP_603	m72[32A6]
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C3421	CAP_603	m72[34C3]
C3430	CAP_402	m72[34B7]
C3431	CAP_402	m72[34B7]
C3700	CAP_603	m72[37D6]
C3701	CAP_402	m72[37D6]
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C3708	CAP_402	m72[37D3]
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C3711	CAP_402	m72[37D6]
C3712	CAP_402	m72[37D5]
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C3714	CAP_402	m72[37D5]
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C3720	CAP_603	m72[37C5]
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C3724	CAP_402	m72[37C4]
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C3735	CAP_402	m72[37C5]
C3736	CAP_402	m72[37C5]
C3740	CAP_402	m72[37B7]
C3742	CAP_402	m72[37B6]
C3744	CAP_402	m72[37B6]
C3746	CAP_402	m72[37B5]
C3750	CAP_402	m72[37B5]
C3751	CAP_402	m72[37B5]
C3780	CAP_402	m72[37B2]
C3800	CAP_805-1	m72[38C8]
C3801	CAP_402	m72[38C7]
C3802	CAP_805-1	m72[38C7]
C3803	CAP_603	m72[38C7]
C3804	CAP_402	m72[38C6]
C3805	CAP_603	m72[38C5]
C3806	CAP_402	m72[38C5]
C3807	CAP_805-1	m72[38C5]
C3810	CAP_805-1	m72[38B6]
C3811	CAP_402	m72[38B6]
C3812	CAP_805-1	m72[38B6]
C3813	CAP_603	m72[38B5]
C3814	CAP_402	m72[38B5]
C3815	CAP_603	m72[38A4]
C3816	CAP_402	m72[38A4]
C3817	CAP_805-1	m72[38A4]
C3890	CAP_402	m72[38C2]
C3891	CAP_402	m72[38C2]
C3900	CAP_402	m72[39D7]
C3901	CAP_402	m72[39D6]
C3910	CAP_1808	m72[39A4]
C4000	CAP_402	m72[40B7]
C4001	CAP_402	m72[40B7]
C4010	CAP_402	m72[40C2]
C4011	CAP_402	m72[40C2]
C4020	CAP_402	m72[40C3]
C4021	CAP_402	m72[40C3]
C4090	CAP_402	m72[40B6]
C4200	CAP_402-LF	m72[42C7]
C4201	CAP_402-LF	m72[42C7]
C4210	CAP_402	m72[42C6]
C4211	CAP_402	m72[42C5]
C4212	CAP_805-1	m72[42C5]
C4213	CAP_805-1	m72[42C5]
C4230	CAP_402	m72[42A5]
C4231	CAP_402	m72[42A5]
C4240	CAP_402	m72[42A7]
C4241	CAP_402	m72[42A7]
C4242	CAP_402	m72[42A7]
C4250	CAP_402	m72[42B7]
C4251	CAP_402	m72[42B7]
C4252	CAP_402	m72[42B7]
C4253	CAP_402	m72[42B6]
C4254	CAP_402	m72[42B6]
C4260	CAP_402	m72[42B7]
C4261	CAP_402	m72[42B7]
C4262	CAP_402	m72[42B7]
C4263	CAP_402	m72[42B6]
C4264	CAP_402	m72[42B6]
C4265	CAP_402	m72[42B6]
C4266	CAP_402	m72[42B6]
C4280	CAP_402	m72[42A6]
C4281	CAP_402	m72[42A6]
C4290	CAP_402	m72[42B5]
C4291	CAP_402	m72[42B5]
C4300	CAP_603-1	m72[43D3]
C4301	CAP_603-1	m72[43B3]
C4310	CAP_402	m72[43D4]
C4311	CAP_402	m72[43D4]
C4312	CAP_402	m72[43C4]
C4313	CAP_402	m72[43C4]
C4320	CAP_402	m72[43B5]
C4321	CAP_402	m72[43B5]
C4322	CAP_402	m72[43A5]
C4323	CAP_402	m72[43A5]
C4332	CAP_402	m72[43C2]
C4335	CAP_603-1	m72[43C2]
C4350	CAP_402	m72[43C7]
C4354	CAP_402	m72[43B7]
C4360	CAP_402	m72[43D7]
C4364	CAP_402	m72[43B7]
C4404	CAP_402	m72[44B6]
C4405	CAP_402	m72[44B4]
C4406	CAP_805	m72[44B4]
C4510	CAP_402	m72[45D6]
C4511	CAP_402	m72[45D6]
C4515	CAP_402	m72[45C6]
C4516	CAP_402	m72[45C6]
C4600	CAP_P_CASE-D2-LF	m72[46C8]
C4613	CAP_402	m72[46D2]
C4623	CAP_402	m72[46C5]
C4633	CAP_402	m72[46A5]
C4650	CAP_402	m72[46D5]
C4700	CAP_805-1	m72[47D7]
C4701	CAP_402	m72[47D6]
C4720	CAP_805-1	m72[47D3]
C4721	CAP_402	m72[47D3]
C4902	CAP_805	m72[49D4]
C4903	CAP_402	m72[49D4]
C4904	CAP_402	m72[49D3]
C4905	CAP_402	m72[49D3]
C4906	CAP_402	m72[49D3]
C4907	CAP_402	m72[49D2]
C4920	CAP_402	m72[49C3]
C5000	CAP_402	m72[50D7]
C5001	CAP_402	m72[50D7]
C5010	CAP_402	m72[50C6]
C5020	CAP_402	m72[50C7]
C5021	CAP_402	m72[50C7]
C5050	CAP_402	m72[50B6]
C5051	CAP_402	m72[50A4]
C5052	CAP_402	m72[50A4]
C5065	CAP_402	m72[50B8]
C5066	CAP_603	m72[50B7]
C5067	CAP_402	m72[50B7]
C5309	CAP_402	m72[53D6]
C5358	CAP_402	m72[53C2]
C5359	CAP_402	m72[53D3]
C5370	CAP_402	m72[53C7]
C5500	CAP_402	m72[55C7]
C5501	CAP_402	m72[55B4]
C5502	CAP_805-1	m72[55B4]
C5503	CAP_402	m72[55B4]
C5510	CAP_402	m72[55A7]
C5511	CAP_402	m72[55A6]
C5550	CAP_402	m72[55B7]
C5551	CAP_402	m72[55B6]
C5570	CAP_402	m72[55C4]
C5580	CAP_402	m72[55C5]
C5601	CAP_805	m72[56D5]
C5602	CAP_P_6.3X5.5SM1	m72[56C4]
C5603	CAP_805	m72[56B5]
C5605	CAP_P_6.3X5.5SM1	m72[56B3]
C5701	CAP_805	m72[57C5]
C5702	CAP_P_6.3X5.5SM1	m72[57C3]
C5880	CAP_402	m72[58C5]
C5881	CAP_402	m72[58D5]
C6100	CAP_402	m72[61C4]
C7000	CAP_402	m72[70C6]
C7001	CAP_402	m72[70C6]
C7002	CAP_402	m72[70C6]
C7003	CAP_402	m72[70C6]
C7010	CAP_603	m72[70D6]
C7052	CAP_402	m72[70D2]
C7056	CAP_402	m72[70D1]
C7060	CAP_402	m72[70A5]
C7061	CAP_402	m72[70B5]
C7062	CAP_402	m72[70B5]
C7090	CAP_402	m72[70A3]
C7100	CAP_402	m72[71C4]
C7101	CAP_1206-1	m72[71D1]
C7102	CAP_402	m72[71B4]
C7103	CAP_402	m72[71C2]
C7104	CAP_402	m72[71B2]
C7105	CAP_402	m72[71C8]
C7106	CAP_402	m72[71B8]
C7107	CAP_402	m72[71B7]
C7108	CAP_1206-1	m72[71D1]
C7109	CAP_P_TH	m72[71D5]
C7110	CAP_402	m72[71C7]
C7111	CAP_402	m72[71B2]
C7112	CAP_402	m72[71C2]
C7113	CAP_402	m72[71B7]
C7114	CAP_402	m72[71B8]
C7115	CAP_603	m72[71D4]
C7116	CAP_402	m72[71B4]
C7121	CAP_402	m72[71A5]
C7126	CAP_603-1	m72[71D6]
C7127	CAP_603	m72[71C4]
C7128	CAP_402	m72[71B4]
C7129	CAP_402	m72[71B5]
C7130	CAP_402	m72[71D6]
C7131	CAP_402	m72[71B5]
C7132	CAP_402	m72[71A5]
C7133	CAP_402	m72[71A5]
C7134	CAP_402	m72[71B5]
C7135	CAP_603	m72[71D4]
C7136	CAP_603	m72[71C4]
C7150	CAP_1206-1	m72[71D4]
C7152	CAP_1206-1	m72[71D4]
C7154	CAP_P_TH	m72[71D2]
C7155	CAP_1206-1	m72[71D1]
C7156	CAP_1206-1	m72[71D4]
C7190	CAP_402	m72[71C3]
C7192	CAP_402	m72[71B3]
C7196	CAP_402	m72[71D6]
C7200	CAP_402	m72[72C4]
C7201	CAP_1206-1	m72[72D2]
C7203	CAP_402	m72[72C2]
C7208	CAP_1206-1	m72[72D2]
C7212	CAP_402	m72[72C3]
C7215	CAP_603	m72[72C5]
C7235	CAP_603	m72[72D6]
C7254	CAP_P_TH	m72[72D2]
C7255	CAP_1206-1	m72[72D2]
C7290	CAP_402	m72[72C4]
C7300	CAP_P_CASE-D2-SM	m72[73C8]
C7301	CAP_805	m72[73C8]
C7302	CAP_402	m72[73B7]
C7303	CAP_P_CASE-D2-SM	m72[73C7]
C7304	CAP_805	m72[73C8]
C7310	CAP_603	m72[73C7]
C7324	CAP_402	m72[73B7]
C7330	CAP_603-1	m72[73D6]
C7331	CAP_603	m72[73C6]

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C7332	CAP_402	m72[73B5]
C7335	CAP_402	m72[73B6]
C7340	CAP_P_TH	m72[73D7]
C7341	CAP_1206-1	m72[73D7]
C7342	CAP_1206-1	m72[73D6]
C7345	CAP_402	m72[73B3]
C7360	CAP_603	m72[73D2]
C7361	CAP_603	m72[73C2]
C7364	CAP_402	m72[73B2]
C7370	CAP_402	m72[73B2]
C7372	CAP_402	m72[73B4]
C7381	CAP_1206-1	m72[73D2]
C7382	CAP_1206-1	m72[73D2]
C7390	CAP_P_CASE-D2-SM	m72[73C1]
C7391	CAP_P_CASE-D2-SM	m72[73C2]
C7392	CAP_805	m72[73C1]
C7393	CAP_805	m72[73C1]
C7400	CAP_P_CASE-D2-SM	m72[74C8]
C7401	CAP_805	m72[74C8]
C7402	CAP_402	m72[74B7]
C7403	CAP_P_CASE-D2-SM	m72[74C7]
C7404	CAP_805	m72[74C8]
C7410	CAP_603	m72[74C7]
C7424	CAP_402	m72[74B7]
C7430	CAP_603-1	m72[74D6]
C7431	CAP_603	m72[74C6]
C7432	CAP_402	m72[74B5]
C7435	CAP_402	m72[74B6]
C7440	CAP_P_TH	m72[74D7]
C7441	CAP_1206-1	m72[74D7]
C7442	CAP_1206-1	m72[74D6]
C7445	CAP_402	m72[74B3]
C7460	CAP_603-1	m72[74D2]
C7461	CAP_603	m72[74C2]
C7464	CAP_402	m72[74B2]
C7470	CAP_402	m72[74B2]
C7472	CAP_402	m72[74B4]
C7480	CAP_P_TH	m72[74D3]
C7481	CAP_1206-1	m72[74D2]
C7482	CAP_1206-1	m72[74D2]
C7490	CAP_P_TH	m72[74C2]
C7491	CAP_P_TH	m72[74C1]
C7492	CAP_805	m72[74C1]
C7493	CAP_805	m72[74C1]
C7500	CAP_603	m72[75D5]
C7501	CAP_603	m72[75D6]
C7502	CAP_603	m72[75D6]
C7503	CAP_402	m72[75C2]
C7506	CAP_402	m72[75C8]
C7507	CAP_402	m72[75C6]
C7508	CAP_603	m72[75C7]
C7509	CAP_402	m72[75D4]
C7510	CAP_402	m72[75C5]
C7530	CAP_P_TH	m72[75D5]
C7531	CAP_603	m72[75D4]
C7532	CAP_P_TH	m72[75D5]
C7533	CAP_1206-1	m72[75D5]
C7534	CAP_1206-1	m72[75D4]
C7540	CAP_805	m72[75C3]
C7541	CAP_805	m72[75C3]
C7542	CAP_P_CASE-D2-SM	m72[75C2]
C7543	CAP_P_CASE-D2-SM	m72[75C2]
C7544	CAP_P_CASE-D2-SM	m72[75C2]
C7550	CAP_402	m72[75B4]
C7551	CAP_805-1	m72[75A6]
C7552	CAP_805-1	m72[75A4]
C7553	CAP_402	m72[75A6]
C7555	CAP_P_CASE-C3	m72[75A4]
C7559	CAP_603	m72[75B5]
C7560	CAP_402	m72[75D8]
C7564	CAP_402	m72[75C3]
C7600	CAP_603	m72[76C4]
C7601	CAP_603	m72[76A4]
C7602	CAP_402	m72[76A4]
C7604	CAP_402	m72[76A3]
C7605	CAP_402	m72[76B5]
C7607	CAP_402	m72[76A3]
C7608	CAP_402	m72[76D2]
C7609	CAP_402	m72[76D7]
C7612	CAP_603	m72[76A7]
C7613	CAP_402	m72[76A7]
C7621	CAP_402	m72[76B6]
C7622	CAP_402	m72[76C5]
C7624	CAP_402	m72[76C6]
C7625	CAP_402	m72[76B6]
C7626	CAP_402	m72[76B6]
C7628	CAP_402	m72[76B7]
C7629	CAP_402	m72[76B7]
C7630	CAP_402	m72[76A5]
C7631	CAP_402	m72[76C7]
C7632	CAP_402	m72[76C2]
C7640	CAP_1206-1	m72[76D6]
C7641	CAP_1206-1	m72[76D6]
C7642	CAP_1206-1	m72[76D6]
C7643	CAP_1206-1	m72[76D6]
C7650	CAP_805	m72[76B7]
C7651	CAP_P_CASE-D3L	m72[76B8]
C7652	CAP_P_CASE-D3L	m72[76B8]
C7661	CAP_402	m72[76B3]
C7662	CAP_402	m72[76C4]
C7664	CAP_402	m72[76C3]
C7665	CAP_402	m72[76B4]
C7666	CAP_402	m72[76B3]
C7668	CAP_402	m72[76B2]
C7669	CAP_402	m72[76B2]
C7670	CAP_402	m72[76B4]
C7680	CAP_1206-1	m72[76D3]
C7681	CAP_1206-1	m72[76D4]
C7682	CAP_P_SM-1	m72[76D4]
C7689	CAP_402	m72[76B4]
C7690	CAP_805	m72[76B2]
C7691	CAP_P_CASE-D3L	m72[76B1]
C7692	CAP_P_CASE-D3L	m72[76B1]
C7693	CAP_P_CASE-D3L	m72[76B1]
C7700	CAP_805	m72[77C6]
C7701	CAP_402	m72[77C5]
C7702	CAP_402	m72[77B3]
C7705	CAP_805	m72[77B3]
C7706	CAP_805	m72[77B3]
C7710	CAP_805	m72[77D6]
C7712	CAP_402	m72[77D4]
C7715	CAP_805	m72[77D3]
C7800	CAP_402	m72[78D4]
C7801	CAP_402	m72[78D4]
C7810	CAP_402	m72[78D6]
C7811	CAP_402	m72[78D7]
C7850	CAP_402	m72[78C4]
C7851	CAP_402	m72[78C4]
C7890	CAP_805	m72[78D2]
C7891	CAP_402	m72[78D2]
C7895	CAP_402	m72[78B7]
C7896	CAP_402	m72[78A6]
C7899	CAP_402	m72[78B6]
C8400	CAP_P_SM-LF	m72[84C5]
C8401	CAP_805	m72[84C7]
C8420	CAP_402	m72[84C7]
C8421	CAP_402	m72[84C7]
C8422	CAP_402	m72[84C7]
C8423	CAP_402	m72[84C7]
C8424	CAP_402	m72[84B7]
C8425	CAP_402	m72[84B7]
C8426	CAP_402	m72[84B7]
C8427	CAP_402	m72[84B7]
C8428	CAP_402	m72[84B7]
C8429	CAP_402	m72[84B7]
C8430	CAP_402	m72[84B7]
C8431	CAP_402	m72[84B7]
C8432	CAP_402	m72[84B7]
C8433	CAP_402	m72[84B7]
C8434	CAP_402	m72[84B7]
C8435	CAP_402	m72[84B7]
C8436	CAP_402	m72[84B7]
C8437	CAP_402	m72[84B7]
C8438	CAP_402	m72[84B7]
C8439	CAP_402	m72[84B7]
C8440	CAP_402	m72[84B7]
C8441	CAP_402	m72[84A7]
C8442	CAP_402	m72[84A7]
C8443	CAP_402	m72[84A7]
C8444	CAP_402	m72[84A7]
C8445	CAP_402	m72[84A7]
C8446	CAP_402	m72[84A7]
C8447	CAP_402	m72[84A7]
C8448	CAP_402	m72[84A7]
C8449	CAP_402	m72[84A7]
C8450	CAP_402	m72[84A7]
C8451	CAP_402	m72[84A7]
C8500	CAP_805	m72[85A5]
C8570	CAP_402	m72[85D2]
C9000	CAP_603-1	m72[90C7]
C9001	CAP_402	m72[90C5]
C9010	CAP_402	m72[90A8]
C9020	CAP_1210	m72[90C5]
C9130	CAP_402	m72[91B7]
C9131	CAP_805-1	m72[91B7]
C9140	CAP_402	m72[91A5]
C9141	CAP_402	m72[91B5]
C9142	CAP_402	m72[91B5]
C9143	CAP_402	m72[91A6]
C9144	CAP_402	m72[91B6]
C9145	CAP_402	m72[91B6]
C9160	CAP_402	m72[91B4]
C9161	CAP_402	m72[91B4]
C9162	CAP_402	m72[91A2]
C9163	CAP_402	m72[91A2]
C9410	CAP_603	m72[94C3]
C9411	CAP_402	m72[94D3]
C9413	CAP_402	m72[94C2]
C9414	CAP_402	m72[94C2]
C9800	CAP_805	m72[98C5]
C9801	CAP_402	m72[98C4]
C9802	CAP_402	m72[98C4]
D2185	DIODE_SCHOT_SOT23	m72[21C4]
D2186	DIODE_SCHOT_SOT23	m72[21B4]
D2702	DIODE_SCHOT_6PB_SOT-363	m72[27D8 27D8]
D2800	DIODE_SCHOT_6PB_SOT-363	m72[28D6]
D4390	ZENER_SOT23	m72[43A6]
D4600	DIODE_SCHOT_3P_A_SC-75	m72[46C2]
D4601	DIODE_SCHOT_3P_A_SC-75	m72[46B5]
D4602	DIODE_SCHOT_3P_A_SC-75	m72[46A5]
D5350	DIODE_3P_2NC_SOT23-F	m72[53C2]
D5600	DIODE_SOT23	m72[56C4]
D5601	DIODE_SOT23	m72[56B4]
D5700	DIODE_SOT23	m72[57C4]
D7100	DIODE_SCHOT_SMB	m72[71D2]
D7101	DIODE_SCHOT_SMB	m72[71B2]
D7200	DIODE_SCHOT_SMB	m72[72C3]
D7300	DIODE_SCHOT_5P_TLM83-3	m72[73B6]
D7301	DIODE_SCHOT_SOT23	m72[73C6]
D7373	DIODE_SCHOT_5P_TLM83-3	m72[73B3]
D7374	DIODE_SCHOT_SOT23	m72[73C3]
D7400	DIODE_SCHOT_5P_TLM83-3	m72[74B6]
D7401	DIODE_SCHOT_SOT23	m72[74C6]
D7473	DIODE_SCHOT_5P_TLM83-3	m72[74B3]
D7474	DIODE_SCHOT_SOT23	m72[74C4]
D7520	DIODE_SCHOT_5P_TLM83-3	m72[75C4]
D7600	DIODE_SCHOT_5P_TLM83-3	m72[76B7]
D7601	DIODE_SCHOT_5P_TLM83-3	m72[76B2]
D7624	DIODE_SCHOT_SOD-323	m72[76C6]
D7664	DIODE_SCHOT_SOD-323	m72[76C3]
D7810	DIODE_SCHOT_SOD-123	m72[78D7]
D7890	DIODE_SCHOT_SOD-123	m72[78D2]
D9400	ZENER_CASE425	m72[94C1]
D9410	DIODE_SCHOT_SOD-123	m72[94D6]
DB4300	DIODE_SCHOT_SM	m72[43D7]
DP4310	DIODE_DUAL_6P_SOT-363	m72[43D4 43D3]
DP4311	DIODE_DUAL_6P_SOT-363	m72[43C4 43C3]
DP4320	DIODE_DUAL_6P_SOT-363	m72[43B5 43B4]
DP4321	DIODE_DUAL_6P_SOT-363	m72[43A5 43A4]
DS4599	LED_2.0X1.25MM-SM	m72[45C2]
F4300	FUSE_SM	m72[43D6]
F4310	FUSE_SM	m72[43D6]
F9410	FUSE_805	m72[94D5]
FL4300	FILTER_4P_DLW21H-SM1	m72[43B3]
FL4310	FILTER_4P_DLW21H-SM1	m72[43B3]
J600	CON_M12RT_D2MT_TH1_M-RT-TH	m72[6D7]
J1000	MEROM_BGA-SKT-P	m72[10C3 10D7]
J1000	MEROM_BGA-SKT-P	m72[11D3 11D7]
J1300	CON_F60ST_D_SM1_F-ST-SM	m72[13C4]
J2800	BATTERY_2P_SM	m72[28D8]
J3100	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	m72[31D5]
J3200	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	m72[32D5]
J3400	CON_F52RT_D2MT_SM_F-RT-SM	m72[34C5]
J3900	CON_RJ45_8ANG_D3MT_TH_F-ANG-TH	m72[39C3]
J4300	CON_F9ANG_1394B_D6MT_TH_F-ANG-TH	m72[43C2]
J4301	CON_F6ANG_S3MT_1394A_TH_F-ANG-TH	m72[43B2]
J4401	CON_M50RT_D2MT_SM_M-RT-SM	m72[44C4]
J4510	CON_M7ST_SATA_SM_M-ST-SM	m72[45D7]
J4610	CON_F4ANG_S4MT_USB_TH_F-ANG-TH	m72[46D1]
J4620	CON_F4ANG_S4MT_USB_TH_F-ANG-TH	m72[46B4]
J4630	CON_F4ANG_S4MT_USB_TH_F-ANG-TH	m72[46A4]
J4700	CON_M6ST_S2MT_SM_M-ST-SM	m72[47B5]
J4720	CON_F10ST_D_SMA_F-ST-SM	m72[47D2]
J5010	CON_M2ST_S2MT_SM_M-S-T-SM	m72[50C6]
J5050	CON_M2ST_S2MT_SM_M-S-T-SM	m72[50A3]
J5100	CON_F30STSM_5047_SM1	m72[51B5]
J5500	CON_M5ST_S2MT_SM_PN1_VD_M-RT-SM	m72[55C7]
J5510	CON_M2ST_S2MT_SM_M-S-T-SM	m72[55A7]
J5511	CON_M2RT_S2MT_SM_M-R-T-SM	m72[55A5]
J5550	CON_M3RT_S2MT_SM_M-R-T-SM	m72[55B7]
J5551	CON_2RTSM_125_SM-2MT-BLK-LF	m72[55B6]
J5600	CON_4SM_WRIB_85205-0401-BLK-ST-SM	m72[56C3]
J5601	CON_M4RT_S2MT_SM_M-R-T-SM	m72[56B2]
J5700	CON_4SM_WRIB_85205-0401-BLK-ST-SM	m72[57C2]
J5880	CON_M7ST_S2MT_SM_M-S-T-SM	m72[58C6]
J8400	CON_F230RT_MXM_SM1_F-RT-SM	m72[84C5]
J8400	CON_F230RT_MXM_SM1_F-RT-SM	m72[85C6]
J9002	CON_F30ST_D_SM_F-ST-SM	m72[90B7]
J9410	CON_DVI_F32ST_Q2MT_SM_F-ST-SM	m72[94D5]
J9800	CON_F20RT_S2MT_SM1_F-RT-SM	m72[98C5]
L2150	IND_0603	m72[21A7]
L2173	IND_1210	m72[21D4]
L2181	IND_0603	m72[21D2]
L2183	IND_0603	m72[21C2]
L2190	IND_0805	m72[21B3]
L2195	IND_0805	m72[21A3]
L2700	IND_0805-1	m72[27C8]
L2702	IND_0805	m72[27A7]
L2703	IND_1210	m72[27A7]
L2901	IND_0402	m72[29D7]
L2902	IND_0402	m72[29D3]
L2903	IND_0402	m72[29C7]
L3800	IND_0805-1	m72[38D7]
L3810	IND_0805-1	m72[38B6]
L4200	IND_0402-LF	m72[42D5]
L4210	IND_0402-LF	m72[42B2]
L4211	IND_0402-LF	m72[42B2]
L4300	IND_SM	m72[43D3]
L4301	IND_SM	m72[43B4]
L4610	IND_SM	m72[46D3]
L4612	FILTER_4P_DLW21H-SM1	m72[46D3]
L4620	IND_SM	m72[46C6]
L4622	FILTER_4P_DLW21H-SM1	m72[46B6]
L4630	IND_SM	m72[46B6]
L4632	FILTER_4P_DLW21H-SM1	m72[46A6]
L4700	IND_SM	m72[47D6]
L4701	FILTER_4P_DLW21H-SM1	m72[47B6]
L4710	FILTER_4P_DLW21H-SM1	m72[47A6]
L5050	IND_3.8X3.8X1.5MM	m72[50A4]
L7100	IND_HM56-11120-TH	m72[71D2]
L7101	IND_HM56-11120-TH	m72[71B2]
L7200	IND_HM56-11120-TH	m72[72C3]
L7300	IND_IHLP2525EZ	m72[73C7]
L7360	IND_IHLP2525EZ	m72[73C2]
L7400	IND_IHLP2525EZ	m72[74C7]
L7460	IND_IHLP5050-MMD12CE-SM	m72[74C2]
L7580	IND_HM56-11121-TH	m72[75C3]
L7620	IND_IHLP2525EZ	m72[76B7]
L7680	IND_HM56-11123-TH	m72[76B2]
L7700	IND_MSCDRI4D28-SM	m72[77B4]
L7710	IND_IHLP	m72[77D4]
L9000	IND_SM	m72[90C6]
L9140	IND_0402	m72[91A5]
L9141	IND_0402	m72[91B5]
L9142	IND_0402	m72[91B5]
L9160	IND_0402	m72[91B2]
L9161	IND_0402	m72[91A2]
L9400	FILTER_4P_SM	m72[94D7]
L9401	FILTER_4P_SM	m72[94D7]
L9402	FILTER_4P_SM	m72[94C7]
L9403	FILTER_4P_SM	m72[94B7]
L9410	IND_SM-1	m72[94D4]
LED601	LED_2.0X1.25MM-SM	m72[6A8]
LED602	LED_2.0X1.25MM-SM	m72[6A7]
LED603	LED_2.0X1.25MM-SM	m72[6A6]
LED604	LED_2.0X1.25MM-SM	m72[6B7]
LED3900	LED_2.0X1.25MM-SM	m72[39A7]
LED3901	LED_2.0X1.25MM-SM	m72[39A7]
LED3902	LED_2.0X1.25MM-SM	m72[39A7]
LED3903	LED_2.0X1.25MM-SM	m72[39A6]
LED4400	LED_2.0X1.25MM-SM	m72[44B5]
PP1000	PROBEPOINT_SM	m72[7D7]
PP1001	PROBEPOINT_SM	m72[7D7]
PP1002	PROBEPOINT_SM	m72[7D7]
PP1003	PROBEPOINT_SM	m72[7D7]
PP1004	PROBEPOINT_SM	m72[7D7]
PP1005	PROBEPOINT_SM	m72[7D7]
PP1006	PROBEPOINT_SM	m72[7D7]
PP1007	PROBEPOINT_SM	m72[7D7]
PP1008	PROBEPOINT_SM	m72[7D7]
PP1009	PROBEPOINT_SM	m72[7D7]
PP1010	PROBEPOINT_SM	m72[7D7]
PP1011	PROBEPOINT_SM	m72[7D7]
PP1012	PROBEPOINT_SM	m72[7D7]
PP1013	PROBEPOINT_SM	m72[7D7]
PP1014	PROBEPOINT_SM	m72[7D7]
PP1015	PROBEPOINT_SM	m72[7D7]
PP1016	PROBEPOINT_SM	m72[7D7]
PP1017	PROBEPOINT_SM	m72[7D7]
PP1018	PROBEPOINT_SM	m72[7D7]
PP1019	PROBEPOINT_SM	m72[7D7]
PP1020	PROBEPOINT_SM	m72[7D7]
PP1021	PROBEPOINT_SM	m72[7C7]
PP1022	PROBEPOINT_SM	m72[7C7]
PP1023	PROBEPOINT_SM	m72[7C7]
PP1024	PROBEPOINT_SM	m72[7C7]
PP1025	PROBEPOINT_SM	m72[7C7]
PP1026	PROBEPOINT_SM	m72[7C7]
PP1027	PROBEPOINT_SM	m72[7C7]
PP1028	PROBEPOINT_SM	m72[7C7]
PP1029	PROBEPOINT_SM	m72[7C7]
PP1030	PROBEPOINT_SM	m72[7C7]
PP1031	PROBEPOINT_SM	m72[7C7]
PP1032	PROBEPOINT_SM	m72[7C7]
PP1033	PROBEPOINT_SM	m72[7C7]
PP1034	PROBEPOINT_SM	m72[7C7]
PP1035	PROBEPOINT_SM	m72[7C7]
PP1400	PROBEPOINT_SM	m72[7D6]
PP1401	PROBEPOINT_SM	m72[7D6]
PP1402	PROBEPOINT_SM	m72[7D6]
PP1403	PROBEPOINT_SM	m72[7D6]
PP1404	PROBEPOINT_SM	m72[7D6]
PP1405	PROBEPOINT_SM	m72[7D6]
PP1406	PROBEPOINT_SM	m72[7D6]
PP1407	PROBEPOINT_SM	m72[7D6]
PP1408	PROBEPOINT_SM	m72[7D6]
PP1409	PROBEPOINT_SM	m72[7D6]
PP1410	PROBEPOINT_SM	m72[7D6]
PP1411	PROBEPOINT_SM	m72[7D6]
PP1412	PROBEPOINT_SM	m72[7D6]
PP1413	PROBEPOINT_SM	m72[7D6]
PP1414	PROBEPOINT_SM	m72[7D6]
PP1415	PROBEPOINT_SM	m72[7D6]
PP1416	PROBEPOINT_SM	m72[7D6]
PP1417	PROBEPOINT_SM	m72[7D6]
PP1418	PROBEPOINT_SM	m72[7D6]
PP1419	PROBEPOINT_SM	m72[7D6]
PP1420	PROBEPOINT_SM	m72[7D6]
PP1421	PROBEPOINT_SM	m72[7C6]
PP1422	PROBEPOINT_SM	m72[7C6]
PP1423	PROBEPOINT_SM	m72[7C6]
PP1424	PROBEPOINT_SM	m72[7C6]
PP1425	PROBEPOINT_SM	m72[7C6]
PP1426	PROBEPOINT_SM	m72[7C6]
PP1427	PROBEPOINT_SM	m72[7C6]
PP1428	PROBEPOINT_SM	m72[7C6]
PP1429	PROBEPOINT_SM	m72[7C6]
PP1430	PROBEPOINT_SM	m72[7C6]
PP1431	PROBEPOINT_SM	m72[7C6]
PP1432	PROBEPOINT_SM	m72[7C6]
PP1433	PROBEPOINT_SM	m72[7C6]
PP1434	PROBEPOINT_SM	m72[7C6]
PP1435	PROBEPOINT_SM	m72[7C6]
PP1436	PROBEPOINT_SM	m72[7C6]
PP1437	PROBEPOINT_SM	m72[7C6]
PP1438	PROBEPOINT_SM	m72[7C6]
PP1439	PROBEPOINT_SM	m72[7C6]
PP1440	PROBEPOINT_SM	m72[7C6]
PP1441	PROBEPOINT_SM	m72[7C6]
PP1442	PROBEPOINT_SM	m72[7C6]
PP1443	PROBEPOINT_SM	m72[7C6]
PP1444	PROBEPOINT_SM	m72[7B6]
PP1445	PROBEPOINT_SM	m72[7B6]
PP1446	PROBEPOINT_SM	m72[7B6]
PP1447	PROBEPOINT_SM	m72[7B6]
PP1448	PROBEPOINT_SM	m72[7B6]
PP1449	PROBEPOINT_SM	m72[7B6]
PP1450	PROBEPOINT_SM	m72[7B6]
PP1451	PROBEPOINT_SM	m72[7B6]
PP1452	PROBEPOINT_SM	m72[7B6]
PP1453	PROBEPOINT_SM	m72[7B6]
PP1454	PROBEPOINT_SM	m72[7B6]
PP1455	PROBEPOINT_SM	m72[7B6]
PP1456	PROBEPOINT_SM	m72[7B6]
PP1457	PROBEPOINT_SM	m72[7B6]
PP1458	PROBEPOINT_SM	m72[7B6]
PP1459	PROBEPOINT_SM	m72[7B6]
PP1460	PROBEPOINT_SM	m72[7B6]
PP1461	PROBEPOINT_SM	m72[7B6]
PP1462	PROBEPOINT_SM	m72[7B6]
PP1463	PROBEPOINT_SM	m72[7B6]
PP1464	PROBEPOINT_SM	m72[7B6]
PP1465	PROBEPOINT_SM	m72[7B6]
PP1466	PROBEPOINT_SM	m72[7B6]
PP1467	PROBEPOINT_SM	m72[7B6]
PP1468	PROBEPOINT_SM	m72[7B6]
PP1469	PROBEPOINT_SM	m72[7B6]
PP1470	PROBEPOINT_SM	m72[7A6]
PP1471	PROBEPOINT_SM	m72[7A6]
PP1472	PROBEPOINT_SM	m72[7A6]
PP1473	PROBEPOINT_SM	m72[7A6]
PP1474	PROBEPOINT_SM	m72[7A6]
PP1475	PROBEPOINT_SM	m72[7A6]
PP1476	PROBEPOINT_SM	m72[7A6]
PP1477	PROBEPOINT_SM	m72[7A6]
PP1478	PROBEPOINT_SM	m72[7A6]
PP1479	PROBEPOINT_SM	m72[7A6]

PP1480	PROBEPOINT_SM	m72[7A6]
PP1481	PROBEPOINT_SM	m72[7A6]
PP1482	PROBEPOINT_SM	m72[7A6]
PP1483	PROBEPOINT_SM	m72[7A6]
PP1484	PROBEPOINT_SM	m72[7A6]
PP1485	PROBEPOINT_SM	m72[7A6]
PP1486	PROBEPOINT_SM	m72[7A6]
PP1487	PROBEPOINT_SM	m72[7A6]
PP1488	PROBEPOINT_SM	m72[7A6]
PP1489	PROBEPOINT_SM	m72[7A6]
PP1490	PROBEPOINT_SM	m72[7A6]
PP1491	PROBEPOINT_SM	m72[7A6]
PP1492	PROBEPOINT_SM	m72[7A6]
PP1493	PROBEPOINT_SM	m72[7A6]
PP2100	PROBEPOINT_SM	m72[7C7]
PP2101	PROBEPOINT_SM	m72[7C7]
PP2102	PROBEPOINT_SM	m72[7C7]
PP2103	PROBEPOINT_SM	m72[7B7]
PP2104	PROBEPOINT_SM	m72[7B7]
PP2105	PROBEPOINT_SM	m72[7B7]
PP2106	PROBEPOINT_SM	m72[7B7]
PP2107	PROBEPOINT_SM	m72[7B7]
PP2108	PROBEPOINT_SM	m72[7B7]
PP2109	PROBEPOINT_SM	m72[7B7]
PP2110	PROBEPOINT_SM	m72[7B7]
PP2111	PROBEPOINT_SM	m72[7B7]
PP2112	PROBEPOINT_SM	m72[7B7]
PP2113	PROBEPOINT_SM	m72[7B7]
PP2114	PROBEPOINT_SM	m72[7B7]
PP2115	PROBEPOINT_SM	m72[7B7]
PP2116	PROBEPOINT_SM	m72[7B7]
PP2117	PROBEPOINT_SM	m72[7B7]
PP2118	PROBEPOINT_SM	m72[7B7]
PP2119	PROBEPOINT_SM	m72[7B7]
PP2120	PROBEPOINT_SM	m72[7B7]
PP2121	PROBEPOINT_SM	m72[7A7]
PP2122	PROBEPOINT_SM	m72[7A7]
PP2123	PROBEPOINT_SM	m72[7A7]
PP2124	PROBEPOINT_SM	m72[7A7]
PP2125	PROBEPOINT_SM	m72[7A7]
PP2126	PROBEPOINT_SM	m72[7A7]
PP2127	PROBEPOINT_SM	m72[7A7]
PP2128	PROBEPOINT_SM	m72[7A7]
PP2129	PROBEPOINT_SM	m72[7A7]
PP2130	PROBEPOINT_SM	m72[7A7]
PP2131	PROBEPOINT_SM	m72[7A7]
PP2132	PROBEPOINT_SM	m72[7B7]
PP2133	PROBEPOINT_SM	m72[7B7]
PP3700	PROBEPOINT_SM	m72[7D5]
PP3701	PROBEPOINT_SM	m72[7D5]
PP3702	PROBEPOINT_SM	m72[7D5]
PP3703	PROBEPOINT_SM	m72[7D5]
PP3704	PROBEPOINT_SM	m72[7D5]
PP4000	PROBEPOINT_SM	m72[7D5]
PP4001	PROBEPOINT_SM	m72[7D5]
PP4002	PROBEPOINT_SM	m72[7D5]
PP4003	PROBEPOINT_SM	m72[7D5]
PP4004	PROBEPOINT_SM	m72[7D5]
PP4900	PROBEPOINT_SM	m72[7C5]
PP4901	PROBEPOINT_SM	m72[7C5]
PP4902	PROBEPOINT_SM	m72[7C5]
PP4903	PROBEPOINT_SM	m72[7C5]
Q600	TRA_2N7002_SOT23-LF	m72[6A8]
Q610	TRA_2N7002_SOT23-LF	m72[6D7]
Q3800	TRA_PBSS5540Z_SOT223	m72[38C5]
Q3810	TRA_PBSS5540Z_SOT223	m72[38A4]
Q4200	TRA_BCP69_SOT223-4	m72[42D6]
Q4600	TRA_2N7002_SOT23-LF	m72[46C8]
Q5050	TRA_DUAL_MMDT3906_SOT-363	m72[50A6 50A7]
Q5052	TRA_2N7002_SOT23-LF	m72[50A8]
Q5077	TRA_DUAL_MMDT3904_SOT-363-LF	m72[50D1 50D2]
Q5095	TRA_2N7002DW_SOT-363	m72[50C2 50C2]
Q5190	TRA_DUAL_MMDT3904_SOT-363-LF	m72[51B3 51C4]
Q5339	TRA_2N7002_SOT23-LF	m72[53B7]
Q5341	TRA_FDC796N_SUPERSOT-6	m72[53B6]
Q5600	TRA_NTHS5443T1_1206A-03-LF	m72[56D4]
Q5602	TRA_2N7002_SOT23-LF	m72[56D6]
Q5603	TRA_NTHS5443T1_1206A-03-LF	m72[56B4]
Q5605	TRA_2N7002_SOT23-LF	m72[56B6]
Q5700	TRA_NTHS5443T1_1206A-03-LF	m72[57D4]
Q5702	TRA_2N7002_SOT23-LF	m72[57C5]
Q7006	TRA_DUAL_SSM6N15FE_SOT563	m72[70A7 70B6]
Q7007	TRA_DUAL_SSM6N15FE_SOT563	m72[70A6 70B6]
Q7100	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m72[71D3]
Q7101	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[71D3]
Q7102	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m72[71C3]
Q7103	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[71B3]
Q7104	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[71C3]
Q7105	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[71B3]
Q7200	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m72[72C4]
Q7201	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[72C4]
Q7204	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[72C3]
Q7300	TRA_FDMS9620S_MLP	m72[73C6]
Q7360	TRA_FDMS9620S_MLP	m72[73C3]
Q7400	TRA_FDMS9620S_MLP	m72[74C6]
Q7460	TRA_FDM6296_MICROFET 3X3	m72[74C3]
Q7461	TRA_FDM6296_MICROFET 3X3	m72[74C3]
Q7520	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m72[75D4]
Q7521	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[75C4]
Q7603	TRA_2N7002_SOT23-LF	m72[76A6]
Q7620	TRA_FDMS9620S_MLP	m72[76C7]
Q7640	TRA_SINGLE_MOSFET_PC HN_SOT-23	m72[53B7]
Q7660	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m72[76C3]
Q7661	TRA_MOSFET_NCHN_5P2_MLP5X6-LFPAK	m72[76B3]
Q7800	TRA_IRF7410_SO-8	m72[78D4]
Q7801	TRA_SINGLE_MOSFET_NC HN_SOT23	m72[78D5]
Q7810	TRA_IRF7410_SO-8	m72[78D7]
Q7811	TRA_SINGLE_MOSFET_NC HN_SOT23	m72[78D8]
Q7850	TRA_IRF7410_SO-8	m72[78C4]
Q7851	TRA_SINGLE_MOSFET_NC HN_SOT23	m72[78C5]
Q7890	TRA_MOSFET_PCHN_8P1_SO1	m72[78D2]
Q7891	TRA_SINGLE_MOSFET_NC HN_SOT23	m72[78C2]
Q7892	TRA_2N7002DW_SOT-363	m72[78C2 78C1]
Q7895	TRA_MOSFET_NCHN_8P_SO-8	m72[78B6]
Q7896	TRA_2N7002_SOT23-LF	m72[78A7]
Q7897	TRA_SINGLE_MOSFET_NC HN_SOT23	m72[78A6]
Q9000	TRA_SI3443DV_TSOP-LF	m72[90C7]
Q9001	TRA_2N7002_SOT23-LF	m72[90B7]
Q9411	TRA_2N7002DW_SOT-363	m72[94D2 94C2]
R600	RES_402	m72[6A7]
R602	RES_402	m72[6A8]
R604	RES_402	m72[6B7]
R605	RES_603	m72[6A6]
R610	RES_402	m72[6D6]
R1002	RES_402	m72[10D5]
R1003	RES_402	m72[10C5]
R1004	RES_402	m72[10C5]
R1005	RES_402	m72[10B5]
R1006	RES_402	m72[10B5]
R1007	RES_402	m72[10A4]
R1012	RES_402	m72[10A4]
R1016	RES_402	m72[10B1]
R1017	RES_402	m72[10B1]
R1018	RES_402	m72[10B1]
R1019	RES_402	m72[10B1]
R1020	RES_402	m72[10B7]
R1021	RES_402	m72[10B7]
R1022	RES_402	m72[10A7]
R1023	RES_402	m72[10A7]
R1024	RES_402	m72[10A7]
R1030	RES_402	m72[10A4]
R1100	RES_402	m72[11B5]
R1101	RES_402	m72[11A5]
R1290	RES_402	m72[12C2]
R1291	RES_402	m72[12C2]
R1292	RES_402	m72[12C2]
R1293	RES_402	m72[12C2]
R1294	RES_402	m72[12C2]
R1295	RES_402	m72[12C2]
R1296	RES_402	m72[12C2]
R1303	RES_402	m72[13B2]
R1315	RES_402	m72[13C6]
R1330	RES_402	m72[13C5]
R1331	RES_402	m72[13C5]
R1399	RES_402	m72[13C7]
R1410	RES_402	m72[14B6]
R1411	RES_402	m72[14A6]
R1415	RES_402	m72[14A6]
R1420	RES_402	m72[14B6]
R1421	RES_402	m72[14B6]
R1425	RES_402	m72[14A7]
R1426	RES_402	m72[14A7]
R1510	RES_402	m72[15D3]
R1610	RES_402	m72[16C2]
R1611	RES_402	m72[16C2]
R1620	RES_402	m72[16C1]
R1622	RES_402	m72[16C1]
R1624	RES_402	m72[16C1]
R1630	RES_402	m72[16B7]
R1631	RES_402	m72[16B7]
R1640	RES_402	m72[16A3]
R1641	RES_402	m72[16A3]
R1655	RES_402	m72[16D7]
R1659	RES_402	m72[16D7]
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R7522	RES_402	m72[75C1]
R7539	RES_402	m72[75D6]
R7551	RES_402	m72[75B5]
R7556	RES_1206	m72[75C3]
R7600	RES_402	m72[76C5]
R7601	RES_402	m72[76A7]
R7602	RES_402	m72[76A7]
R7603	RES_402	m72[76A3]
R7604	RES_402	m72[76A3]
R7606	RES_402	m72[76A4]
R7607	RES_402	m72[76A4]
R7612	RES_402	m72[76A6]
R7613	RES_402	m72[76D7]
R7614	RES_402	m72[76D7]
R7615	RES_402	m72[76D7]
R7616	RES_402	m72[76D7]
R7617	RES_402	m72[76D7]
R7618	RES_402	m72[76D6]
R7621	RES_402	m72[76C7]
R7624	RES_402	m72[76C6]
R7625	RES_402	m72[76B6]
R7626	RES_402	m72[76C7]
R7627	RES_402	m72[76B7]
R7628	RES_402	m72[76B7]
R7629	RES_402	m72[76C7]
R7630	RES_402	m72[76A7]
R7631	RES_402	m72[76A7]
R7661	RES_402	m72[76C2]
R7664	RES_402	m72[76C3]
R7665	RES_402	m72[76B4]
R7666	RES_402	m72[76C2]
R7667	RES_402	m72[76B2]
R7668	RES_402	m72[76B2]
R7669	RES_402	m72[76C2]
R7670	RES_402	m72[76C4]
R7692	RES_402	m72[76A6]
R7700	RES_402	m72[77C6]
R7701	RES_402	m72[77C5]
R7702	RES_402	m72[77B5]
R7703	RES_402	m72[77B3]
R7704	RES_402	m72[77B3]
R7705	RES_402	m72[77B2]
R7710	RES_402	m72[77D6]
R7711	RES_402	m72[77D6]
R7712	RES_402	m72[77D4]
R7713	RES_402	m72[77C4]
R7800	RES_402	m72[78D5]
R7801	RES_402	m72[78D5]
R7810	RES_402	m72[78D8]
R7811	RES_402	m72[78D7]
R7850	RES_402	m72[78C5]
R7851	RES_402	m72[78C5]
R7870	RES_402	m72[78B7]
R7871	RES_402	m72[78B7]
R7888	RES_402	m72[78C1]
R7889	RES_402	m72[78C2]
R7891	RES_402	m72[78D3]
R7892	RES_402	m72[78D2]
R7893	RES_402	m72[78D3]
R7894	RES_805	m72[78D1]
R7895	RES_402	m72[78A7]
R7896	RES_402	m72[78A6]

R7897	RES_402	m72[78B6]
R7898	RES_402	m72[78B6]
R8500	RES_402	m72[85C7]
R8501	RES_402	m72[85C5]
R8502	RES_402	m72[85C7]
R8503	RES_402	m72[85A4]
R8505	RES_402	m72[85B4]
R8570	RES_402	m72[85D3]
R9000	RES_402	m72[90C8]
R9001	RES_402	m72[90C7]
R9002	RES_805	m72[90C8]
R9003	RES_805	m72[90C8]
R9070	RES_402	m72[90B7]
R9074	RES_402	m72[90B2]
R9075	RES_402	m72[90B2]
R9090	RES_805	m72[90C6]
R9099	RES_402	m72[90C8]
R9140	RES_402	m72[91A6]
R9141	RES_402	m72[91B6]
R9142	RES_402	m72[91B6]
R9160	RES_402	m72[91B3]
R9161	RES_402	m72[91A3]
R9400	RES_402	m72[94D7]
R9402	RES_402	m72[94D7]
R9403	RES_402	m72[94D7]
R9404	RES_402	m72[94C7]
R9405	RES_402	m72[94C7]
R9408	RES_402	m72[94C7]
R9409	RES_402	m72[94C7]
R9410	RES_402	m72[94D2]
R9411	RES_402	m72[94D2]
R9412	RES_402	m72[94D2]
R9413	RES_402	m72[94C2]
R9414	RES_402	m72[94C2]
R9415	RES_402	m72[94B7]
R9420	RES_402	m72[94D1]
R9421	RES_402	m72[94D1]
R9422	RES_402	m72[94C2]
RP3300	RPAK4P_SM-LF	m72[33C4 33C4 33C4 33C4]
RP3305	RPAK4P_SM-LF	m72[33B4 33C4 33C4 33C4]
RP3310	RPAK4P_SM-LF	m72[33D4 33A4 33A4 33A4]
RP3330	RPAK4P_SM-LF	m72[33D4 33B4 33B4 33B4]
RP3334	RPAK4P_SM-LF	m72[33B4 33B4 33B4 33B4]
RP3338	RPAK4P_SM-LF	m72[33A4 33B4 33B4 33A4]
RP3342	RPAK4P_SM-LF	m72[33B4 33C4 33C4 33C4]
RP3346	RPAK4P_SM-LF	m72[33D4 33C4 33B4 33C4]
RP3350	RPAK4P_SM-LF	m72[33B4 33A4 33B4 33B4]
RP3354	RPAK4P_SM-LF	m72[33B4 33A4 33A4 33B4]
RP3358	RPAK4P_SM-LF	m72[33C4 33C4 33C4 33C4]
RP3362	RPAK4P_SM-LF	m72[33A4 33C4 33D4 33A4]
S5000	SWI_TACT_4SM_EVQPH_S M-LF	m72[50D8]
S5010	SWI_TACT_4SM_EVQPH_S M-LF	m72[50C7]
SC0700	SPRING_CLIP_1P_EMI_C LIP-SM1	m72[7B6]
SC0701	SPRING_CLIP_1P_EMI_C LIP-SM1	m72[7B5]
SC0702	SPRING_CLIP_1P_EMI_C LIP-SM1	m72[7B5]
SDF0717	PCB_STANDOFF	m72[7A3]
SDF0721	PCB_STANDOFF	m72[7A2]
SDF0724	PCB_STANDOFF	m72[7A6]
SDF0726	HSK_NUT_TH	m72[7A5]
SDF0727	HSK_NUT_TH	m72[7A5]
SDF3400	PCB_STANDOFF	m72[34A5]
SDF4720	PCB_STANDOFF	m72[47D2]
SDF4721	PCB_STANDOFF	m72[47C1]
SDF9000	PCB_STANDOFF	m72[90B7]
SDF9001	PCB_STANDOFF	m72[90A7]
SDF9800	PCB_STANDOFF	m72[98D5]
SDF9801	PCB_STANDOFF	m72[98D5]
SDF9803	PCB_STANDOFF	m72[98B5]
SDF9804	PCB_STANDOFF	m72[98B5]
SW2800	SWI_TACT_4SM_EVQPH_S M-LF	m72[28A4]
T3900	XFR_LFE9245A_SOI	m72[39C5]
U1400	CRESTLINE_FCBGA	m72[14D4]
U1400	CRESTLINE_FCBGA	m72[15D4]
U1400	CRESTLINE_FCBGA	m72[16D5]
U1400	CRESTLINE_FCBGA	m72[17D3 17D7]
U1400	CRESTLINE_FCBGA	m72[18D3 18D7]
U1400	CRESTLINE_FCBGA	m72[19D5]
U1400	CRESTLINE_FCBGA	m72[20D4 20D7]
U2300	SB_ICH8M_BGA	m72[23D5]
U2300	SB_ICH8M_BGA	m72[24B7 24D4]
U2300	SB_ICH8M_BGA	m72[25D4]
U2300	SB_ICH8M_BGA	m72[26D5 26D8]
U2803	MC74VHC1G00_SC70-5	m72[28A7]
U2900	CLK_SYN_SLG8LP537_QF N	m72[29C5]
U3700	88E8058_QFN	m72[37C4]
U3780	EEPROM_M24C08_SO8	m72[37B2]
U4000	FW643_BGA	m72[40C5]
U4600	SWI_TPS2060_MSOP	m72[46C7]
U4601	SWI_TPS2068_MSOP	m72[46D7]
U4650	PI3USB10_TDFN	m72[46D4]
U4900	SMC_H8S2116_BGA	m72[49A3 49C3 49B7 49D7]
U5000	VDET_RN5VD_SOT23-5	m72[50D7]
U5050	MM3120_LLP	m72[50A4]
U5350	ZXCT1010_SOT23-5	m72[53C4]
U5500	LM95214_LLP	m72[55B4]
U5570	EMC1043_MSOP	m72[55C4]
U6100	FLASH_SST25VF016B_SO I_SOI	m72[61C5]
U7010	COMPARATOR_LM339A_SO I-LF	m72[70D6]
U7052	MC74VHC1G08_SOT23-5- LF	m72[70C2]
U7056	MC74VHC1G08_SOT23-5- LF	m72[70C2]
U7100	ISL6260C_QFN	m72[71C6]
U7101	ISL6208_QFN	m72[71D5]
U7102	ISL6208_QFN	m72[71C5]
U7201	ISL6208_QFN	m72[72C7]
U7300	ISL6539_SSOP	m72[73C5]
U7400	ISL6539_SSOP	m72[74C5]
U7500	ISL6269_QFN	m72[75D6]
U7501	SN74LVC1G07_SC70	m72[75D8]
U7550	LREG_BD3533FVM_MSOP- 8	m72[75B4]
U7600	LTC3728L_QFN	m72[76C5]
U7601	COMPARATOR_LM393_SOI -1-LF	m72[76D6 76A7]

U7710	TPS62050_MSOP	m72[77D5]
U7750	TPS62510_BQA	m72[77B4]
U8570	EEPROM_M24C02_SO8	m72[85D2]
U9130	VIDEO_TS3V330_SOP	m72[91B7]
U9160	74LVC1G125LF_SOT23-5	m72[91B4]
U9161	74LVC1G125LF_SOT23-5	m72[91A4]
VR5065	VREF_REF3133_SOT23-3	m72[50B8]
XW4900	SHORT_SM	m72[49C2]
XW5309	SHORT_SM	m72[53D7]
XW5350	SHORT_SM	m72[53C3]
XW5500	SHORT_SM	m72[55A4]
XW5501	SHORT_SM	m72[55A4]
XW5502	SHORT_SM	m72[55A4]
XW5503	SHORT_SM	m72[55A4]
XW7100	SHORT_SM	m72[71A6]
XW7101	SHORT_SM	m72[71B2]
XW7102	SHORT_SM	m72[71B1]
XW7103	SHORT_SM	m72[71D2]
XW7104	SHORT_SM	m72[71D1]
XW7203	SHORT_SM	m72[72C3]
XW7204	SHORT_SM	m72[72C2]
XW7300	SHORT_SM	m72[73B4]
XW7400	SHORT_SM	m72[74B4]
XW7500	SHORT_SM	m72[75C5]
XW7600	SHORT_SM	m72[76A5]
Y2800	CRYSTAL_4PIN_SM-LF	m72[28C7]
Y2901	CRYSTAL_5X3.2-SM	m72[29C6]
Y3750	CRYSTAL_SM-3-LF	m72[37B5]
Y4000	CRYSTAL_HC49-USMD	m72[40B7]
Y5020	CRYSTAL_SM-4	m72[50C8]
ZH500	HOLE_VIA	m72[7C1]
ZH501	HOLE_VIA	m72[7C1]
ZH502	HOLE_VIA	m72[7C1]
ZH503	HOLE_VIA	m72[7C1]
ZH504	HOLE_VIA	m72[7B1]
ZH505	HOLE_VIA	m72[7B1]
ZH506	HOLE_VIA	m72[7B1]
ZH507	HOLE_VIA	m72[7B1]
ZH508	HOLE_VIA	m72[7B1]
ZH509	HOLE_VIA	m72[7B1]
ZH510	HOLE_VIA	m72[7C1]
ZH511	HOLE_VIA	m72[7C1]
ZH512	HOLE_VIA	m72[7C1]
ZH513	HOLE_VIA	m72[7C1]
ZH514	HOLE_VIA	m72[7B1]
ZH515	HOLE_VIA	m72[7B1]
ZH516	HOLE_VIA	m72[7B1]
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ZH518	HOLE_VIA	m72[7B1]
ZH519	HOLE_VIA	m72[7B1]
ZH520	HOLE_VIA	m72[7C1]
ZH521	HOLE_VIA	m72[7C1]
ZH522	HOLE_VIA	m72[7C1]
ZH523	HOLE_VIA	m72[7C1]
ZH524	HOLE_VIA	m72[7B1]
ZH525	HOLE_VIA	m72[7B1]
ZH526	HOLE_VIA	m72[7B1]
ZH527	HOLE_VIA	m72[7B1]
ZH528	HOLE_VIA	m72[7B1]
ZH529	HOLE_VIA	m72[7B1]
ZH0700	MTGHOLE	m72[7A3]
ZH0701	MTGHOLE	m72[7A3]
ZH0702	MTGHOLE	m72[7A3]
ZH0703	MTGHOLE	m72[7A2]
ZH0710	MTGHOLE	m72[7A6]
ZH0711	MTGHOLE	m72[7A5]
ZH0712	MTGHOLE	m72[7A5]
ZH0713	MTGHOLE	m72[7A5]
ZH0714	MTGHOLE	m72[7A4]
ZH0715	MTGHOLE	m72[7A4]
ZH0718	MTGHOLE	m72[7A3]
ZH0719	MTGHOLE	m72[7A3]
ZH0720	MTGHOLE	m72[7A3]
ZH0722	MTGHOLE	m72[7A4]
ZH0723	MTGHOLE	m72[7A4]
ZH0725	MTGHOLE	m72[7A4]

Preliminary